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EP 0411180 A1 WO 91/07813 A1 US 4943783 A

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(54) Amplifier with feedforward and predistortion linearization

(57) An arrangement for linearizing an amplifier by a combination of two methods is described. In the first a predistorter 213 supplies harmonics to the main amplifier 214 in such a way as to counteract the distortion. In the second a feedforward arrangement subtracts in 219 a signal derived from the input of the main amplifier from a signal derived from the output to produce a distortion signal which is then subtracted from the main amplifier output to remove remaining distortion. The arrangement may be used in multi-carrier amplification.

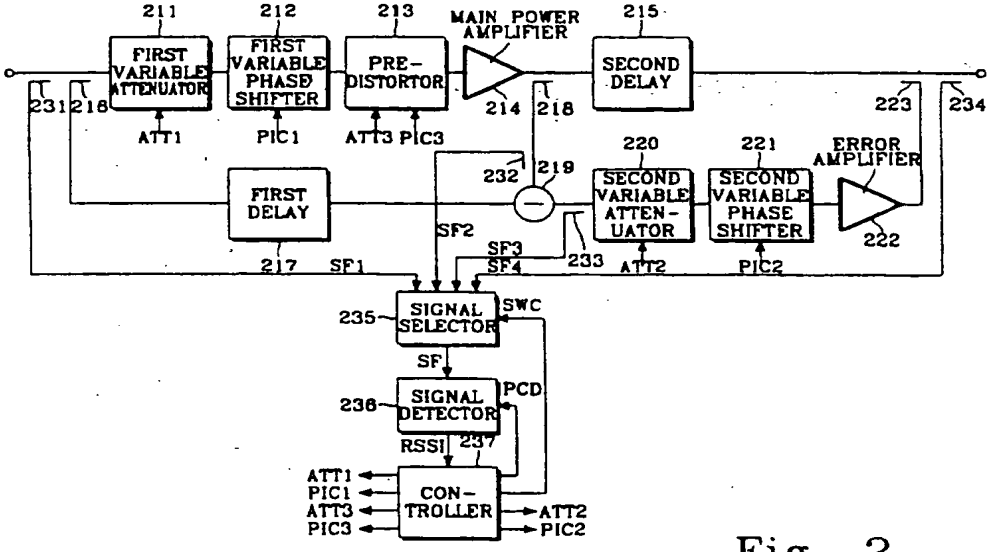
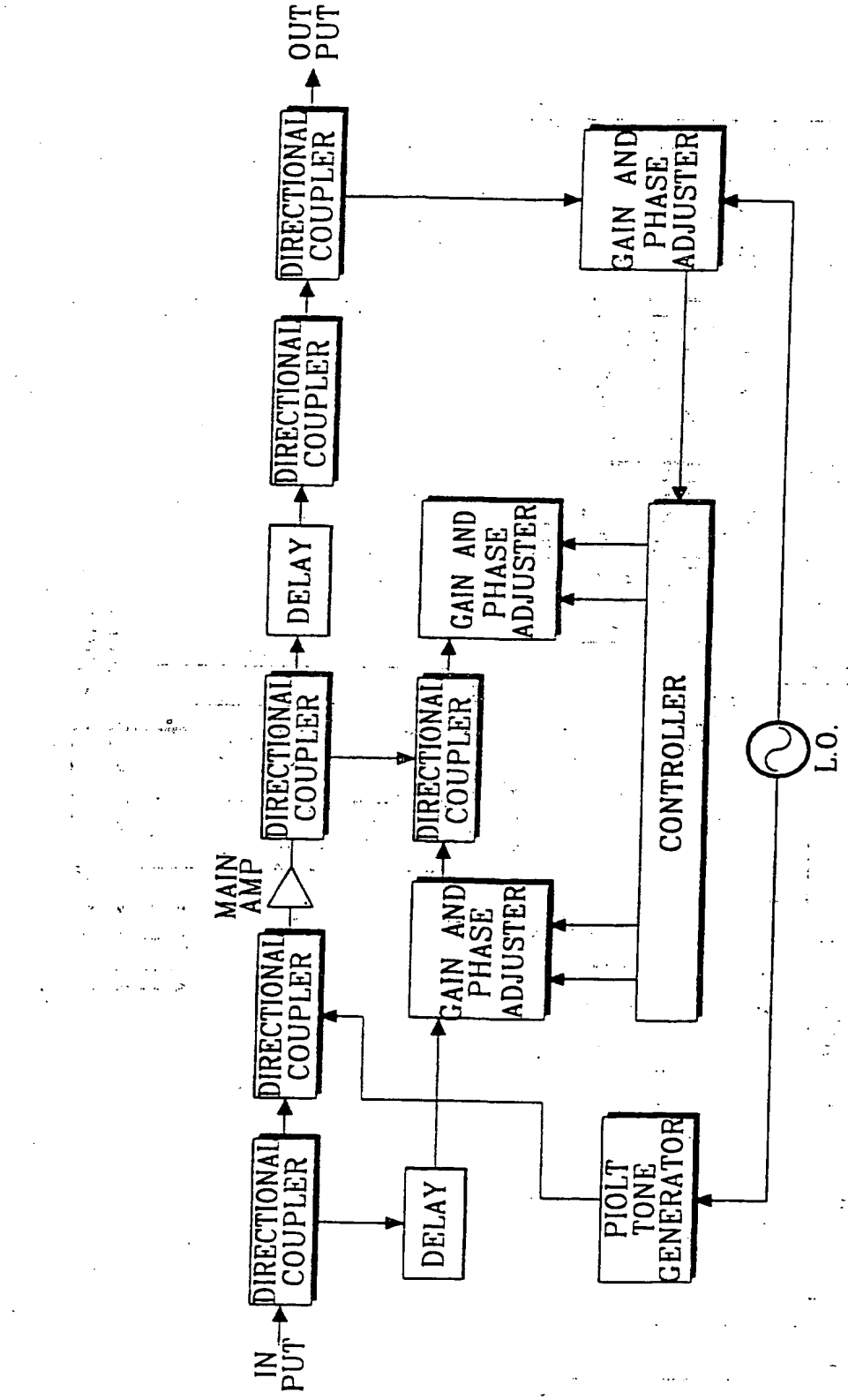


Fig. 2

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

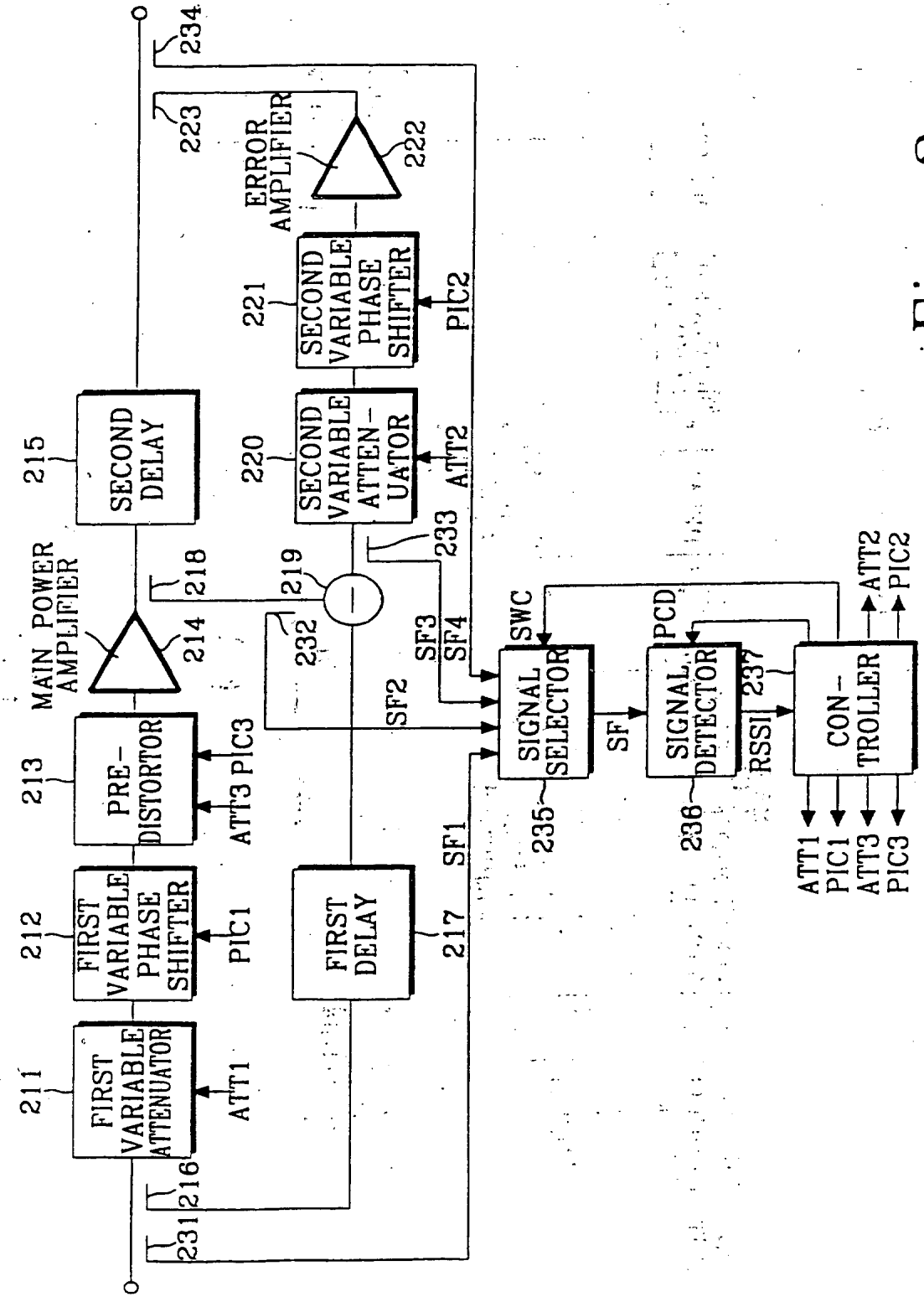
This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1995

GB 2 318 938 A



(PRIOR ART)

Fig. 1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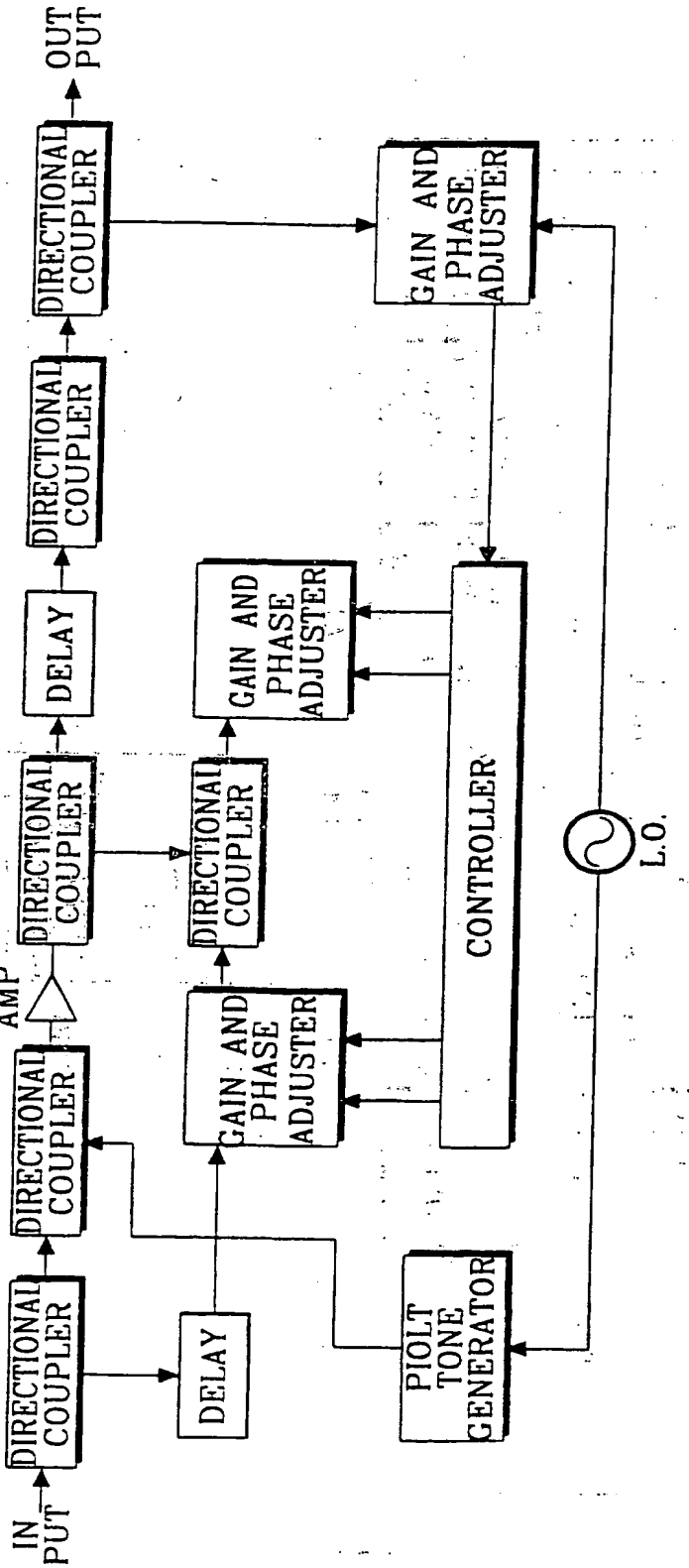
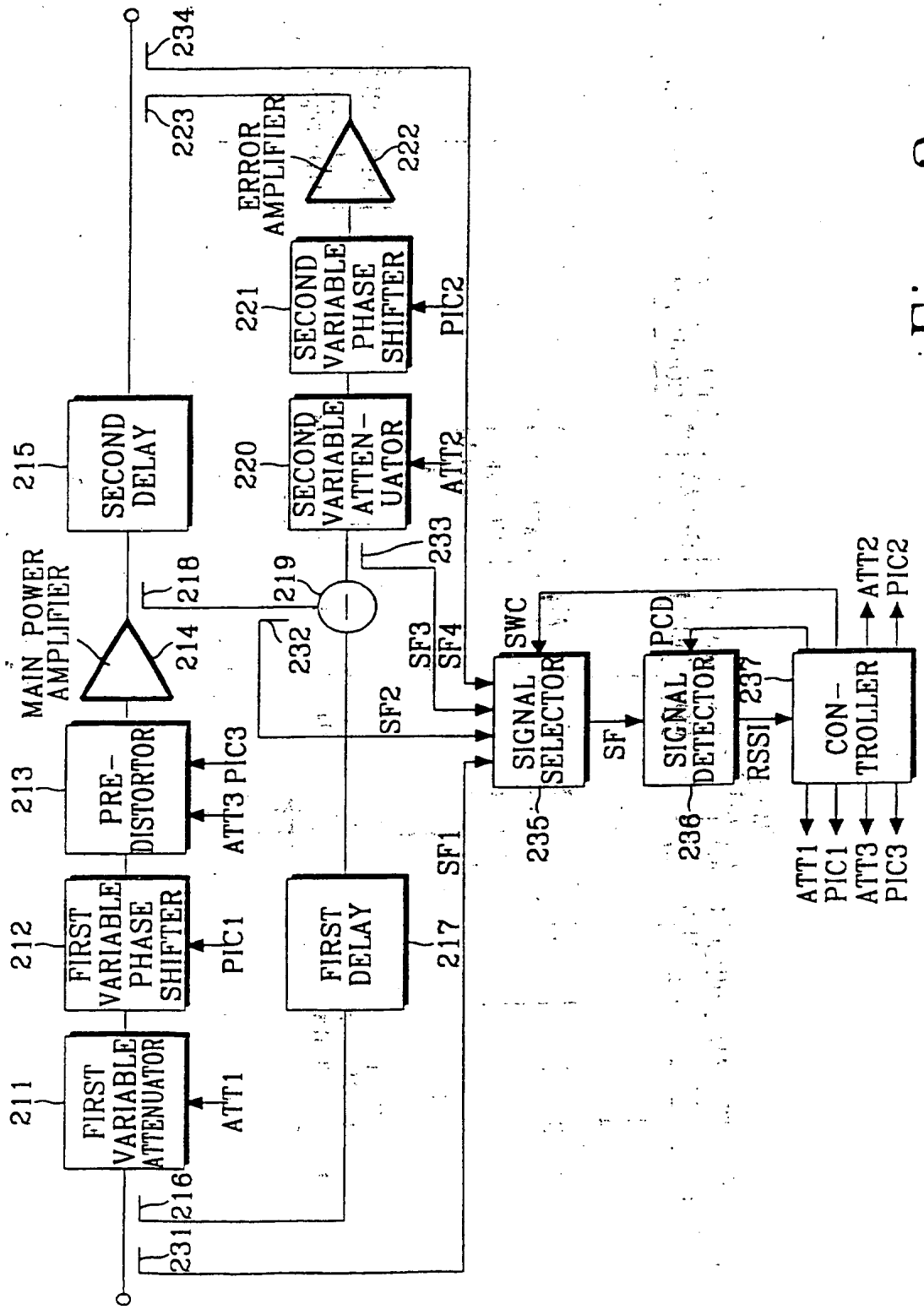
FIRST VARIABLE ATTENUATOR
ATT1
212
FIRST VARIABLE PHASE SHIFTER
PIC1
213
PRE-DISTORTOR
ATT3 PIC3
214
MAIN POWER AMPLIFIER
215
SECOND DELAY
216
218
219
220
SECOND VARIABLE ATTEN-UATOR
ATT2
221
SECOND VARIABLE PHASE SHIFTER
PIC2
222
ERROR AMPLIFIER
223
231
232
233
234
FIRST DELAY
217
SF1
SF2
SF3
SF4
SWC
SIGNAL SELECTOR
235
SF
PCD
SIGNAL DETECTOR
236
RSSI
237
CON-TROLLER
ATT2
PIC2
ATT1
PIC1
ATT3
PIC3

Fig. 2



(PRIOR ART)

Fig. 1


FIRST VARIABLE ATTENUATOR
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ATT1
216
231
FIRST VARIABLE PHASE SHIFTER
212
PIC1
PRE-DISTORTOR
213
ATT3
PIC3
MAIN POWER AMPLIFIER
214
SECOND DELAY
215
218
FIRST DELAY
217
SF1
219
232
SECOND VARIABLE ATTEN-UATOR
220
ATT2
233
SECOND VARIABLE PHASE SHIFTER
221
PIC2
ERROR AMPLIFIER
222
223
234
SF2
SF3
SF4
SWC
SIGNAL SELECTOR
235
SF
SIGNAL DETECTOR
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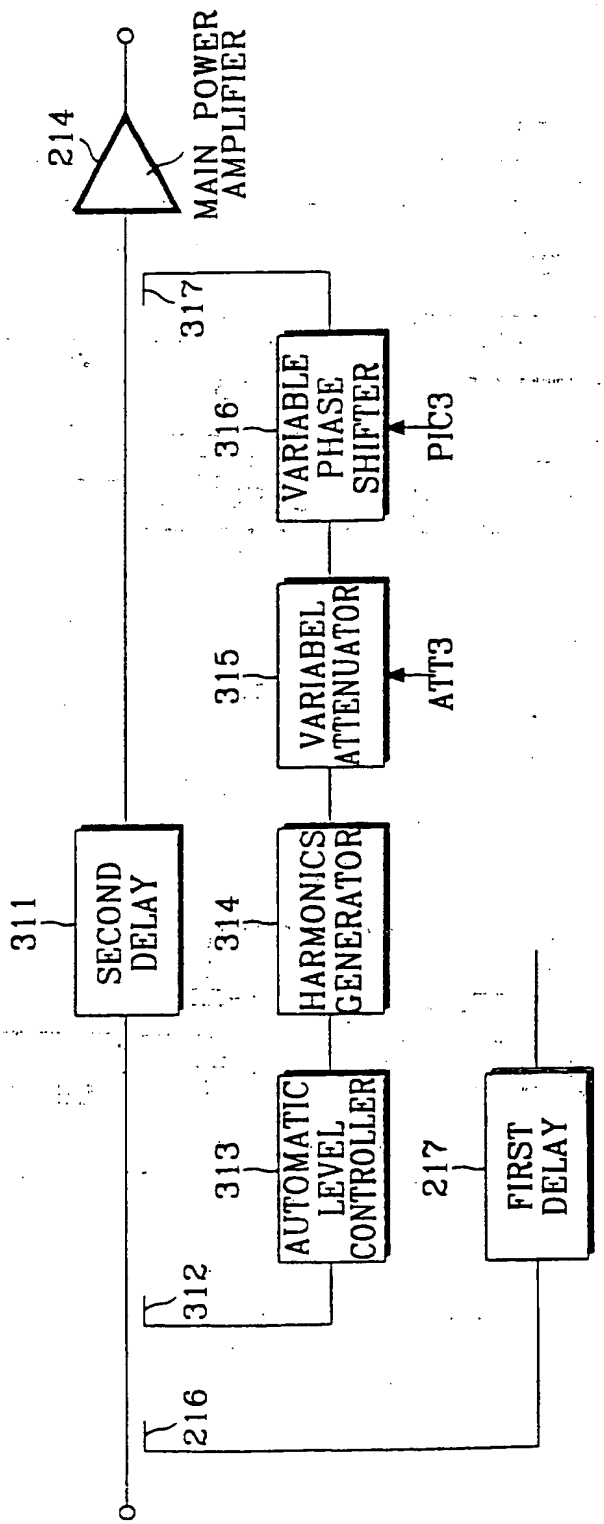
PCD
RSSI
237
CON-TROLLER
ATT1
PIC1
ATT3
PIC3
ATT2
PIC2

Fig. 2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MAIN POWER AMPLIFIER
317
316
VARIABLE PHASE SHIFTER
PIC3
315
VARIABEL ATTENUATOR
ATT3
311
SECOND DELAY
314
HARMONICS GENERATOR
313
AUTOMATIC LEVEL CONTROLLER
217
FIRST DELAY
312
216

Fig. 3

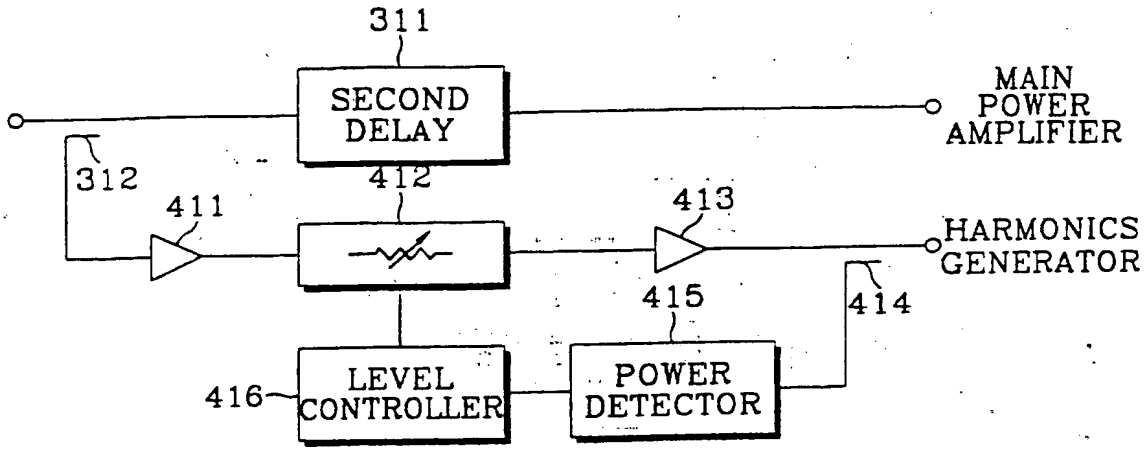

311
SECOND DELAY
MAIN POWER AMPLIFIER
312
412
411
413
HARMONICS GENERATOR
415
414
LEVEL CONTROLLER
416
POWER DETECTOR

Fig. 4

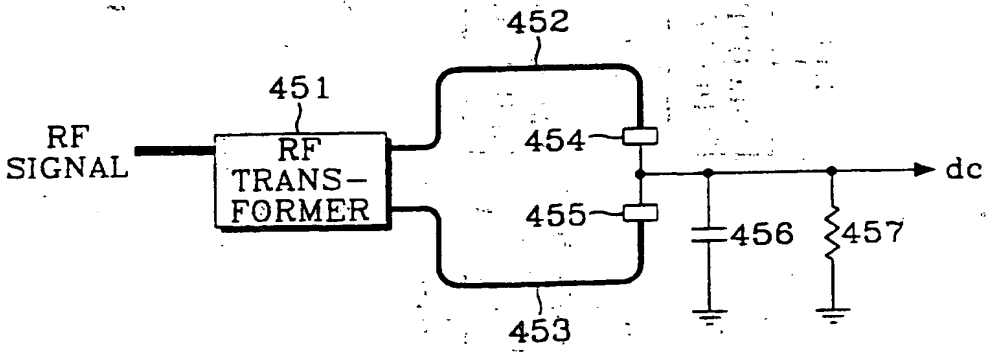

452
451
RF SIGNAL
RF TRANS-FORMER
454
455
dc
456
457
453

Fig. 5

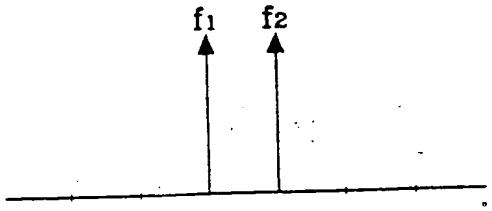


Fig. 6A

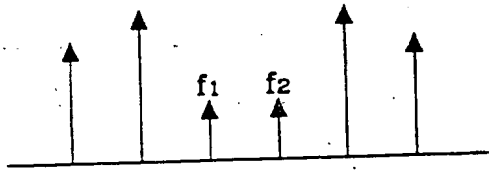


Fig. 6B

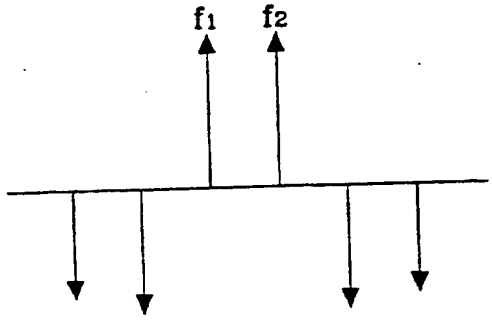


Fig. 6C

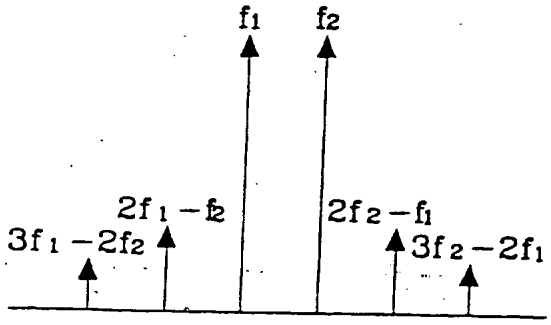


FIG. 6D

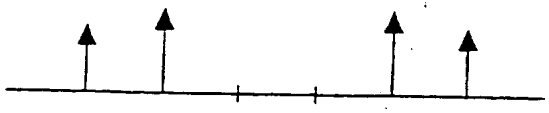


FIG. 6E

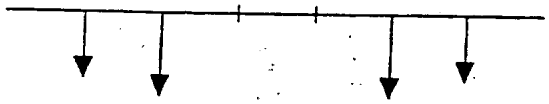


FIG. 6F

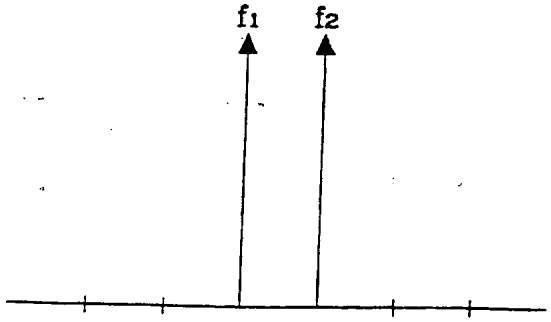


FIG. 6G

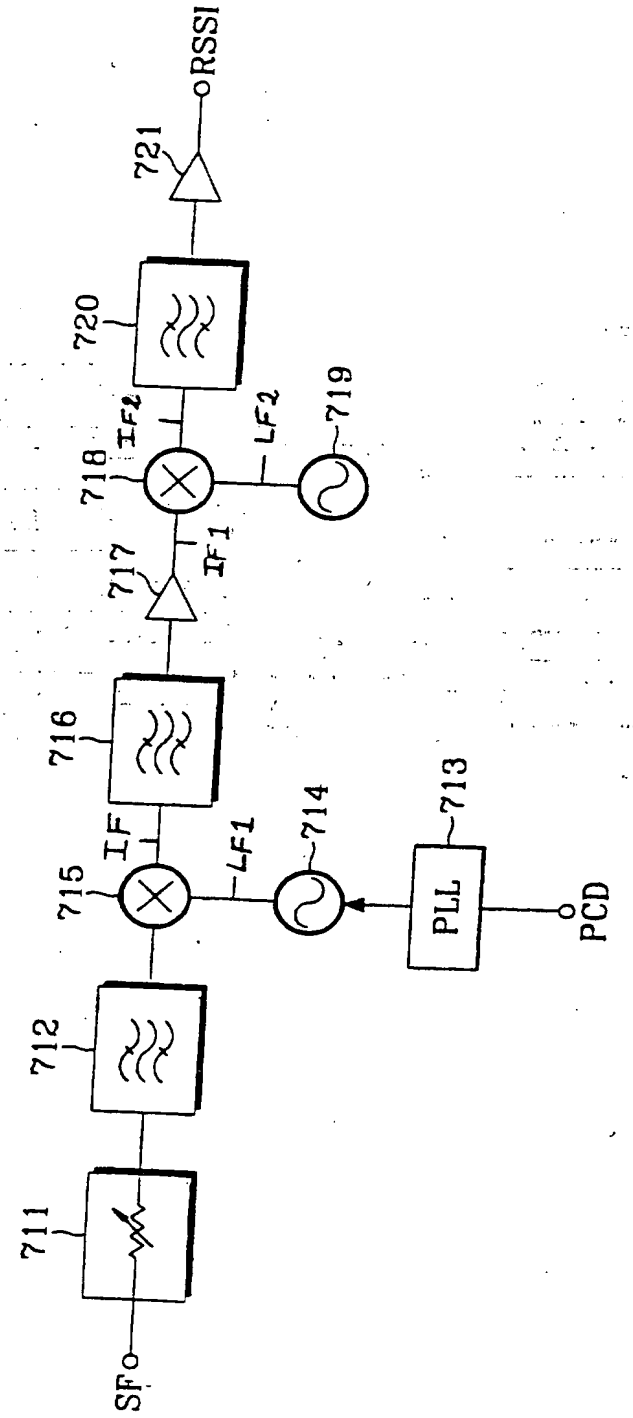
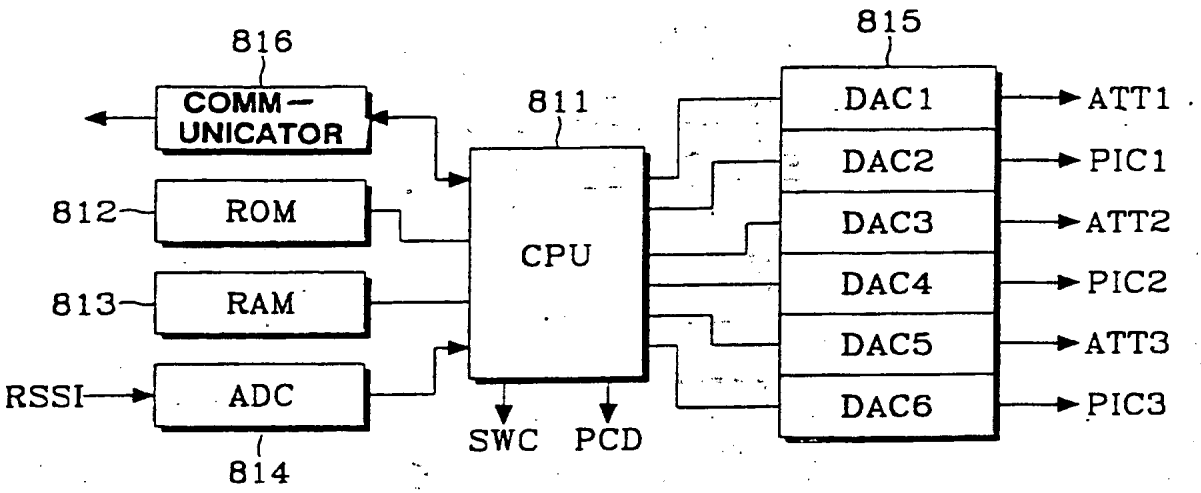

RSSI
721
720
719
IF2
LF2
718
IF1
717
716
IF
LF1
714
713
715
PLL
PCD
712
711
SF

Fig. 7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COMM—
UNICATOR
812
ROM
813
RAM
RSSI
ADC
814
811
CPU
SWC
PCD
815
DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
ATT1
PIC1
ATT2
PIC2
ATT3
PIC3

Fig. 8

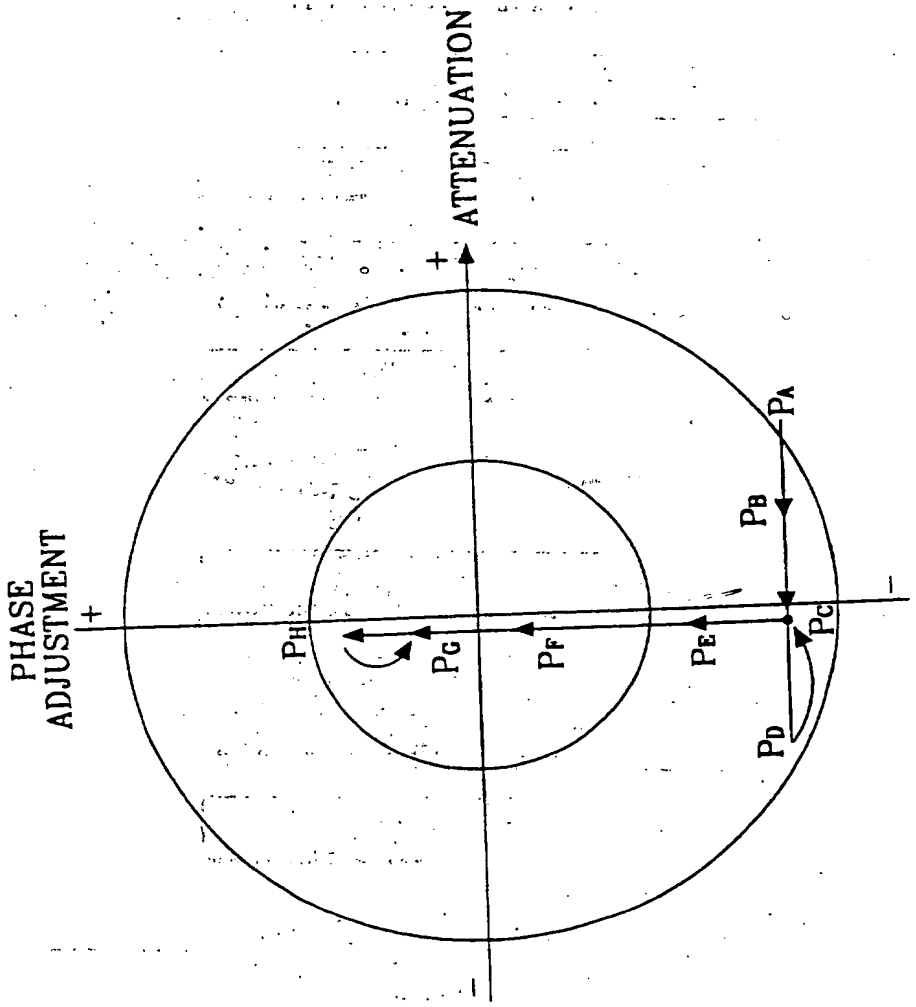


Fig. 9

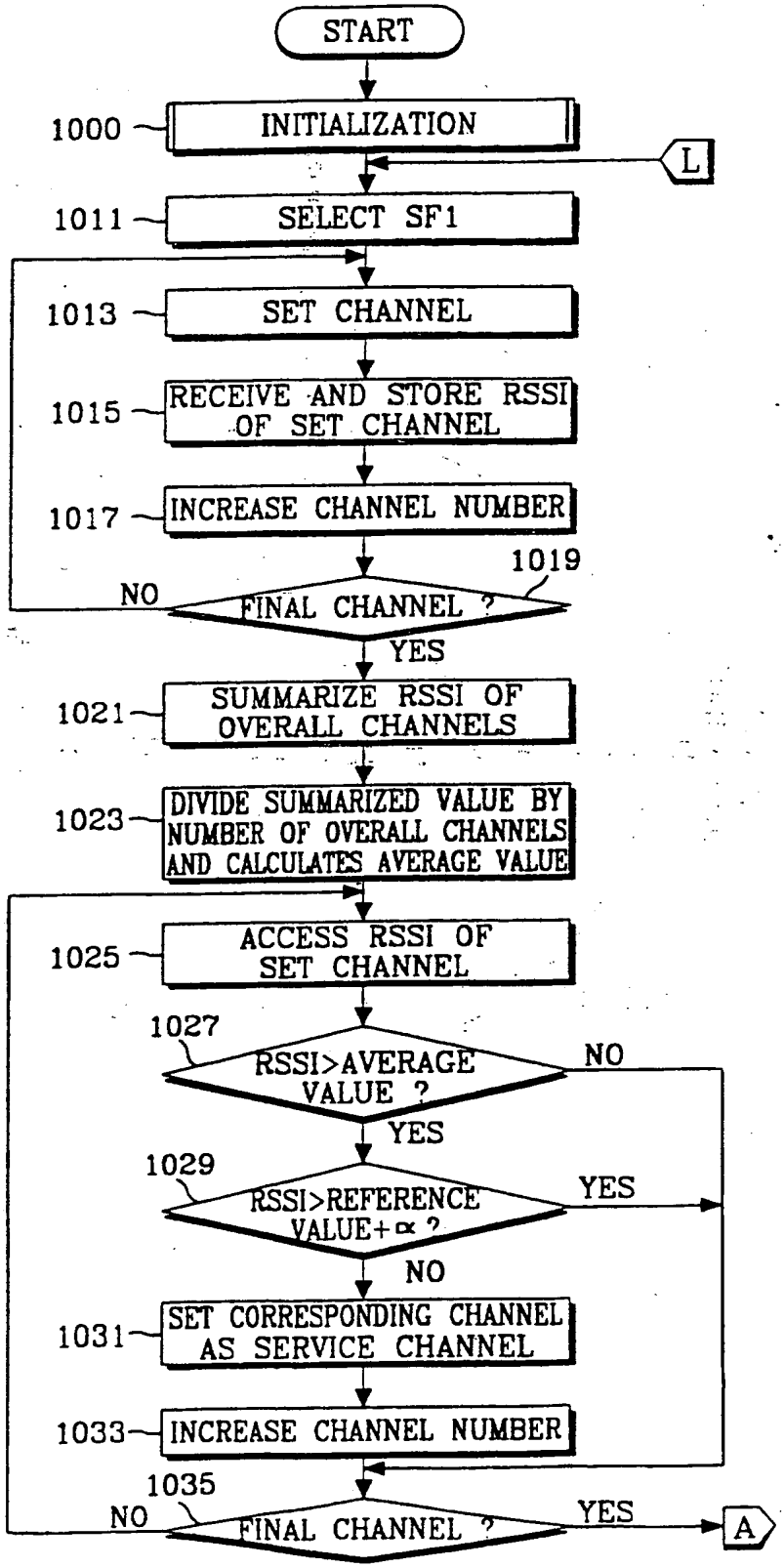

START
1000
INITIALIZATION
L
1011
SELECT SF1
1013
SET CHANNEL
1015
RECEIVE AND STORE RSSI OF SET CHANNEL
1017
INCREASE CHANNEL NUMBER
1019
NO
FINAL CHANNEL ?
YES
1021
SUMMARIZE RSSI OF OVERALL CHANNELS
1023
DIVIDE SUMMARIZED VALUE BY NUMBER OF OVERALL CHANNELS AND CALCULATES AVERAGE VALUE
1025
ACCESS RSSI OF SET CHANNEL
1027
RSSI>AVERAGE VALUE ?
NO
YES
1029
RSSI>REFERENCE VALUE+α ?
YES
NO
1031
SET CORRESPONDING CHANNEL AS SERVICE CHANNEL
1033
INCREASE CHANNEL NUMBER
1035
NO
FINAL CHANNEL ?
YES
A

Fig. 10

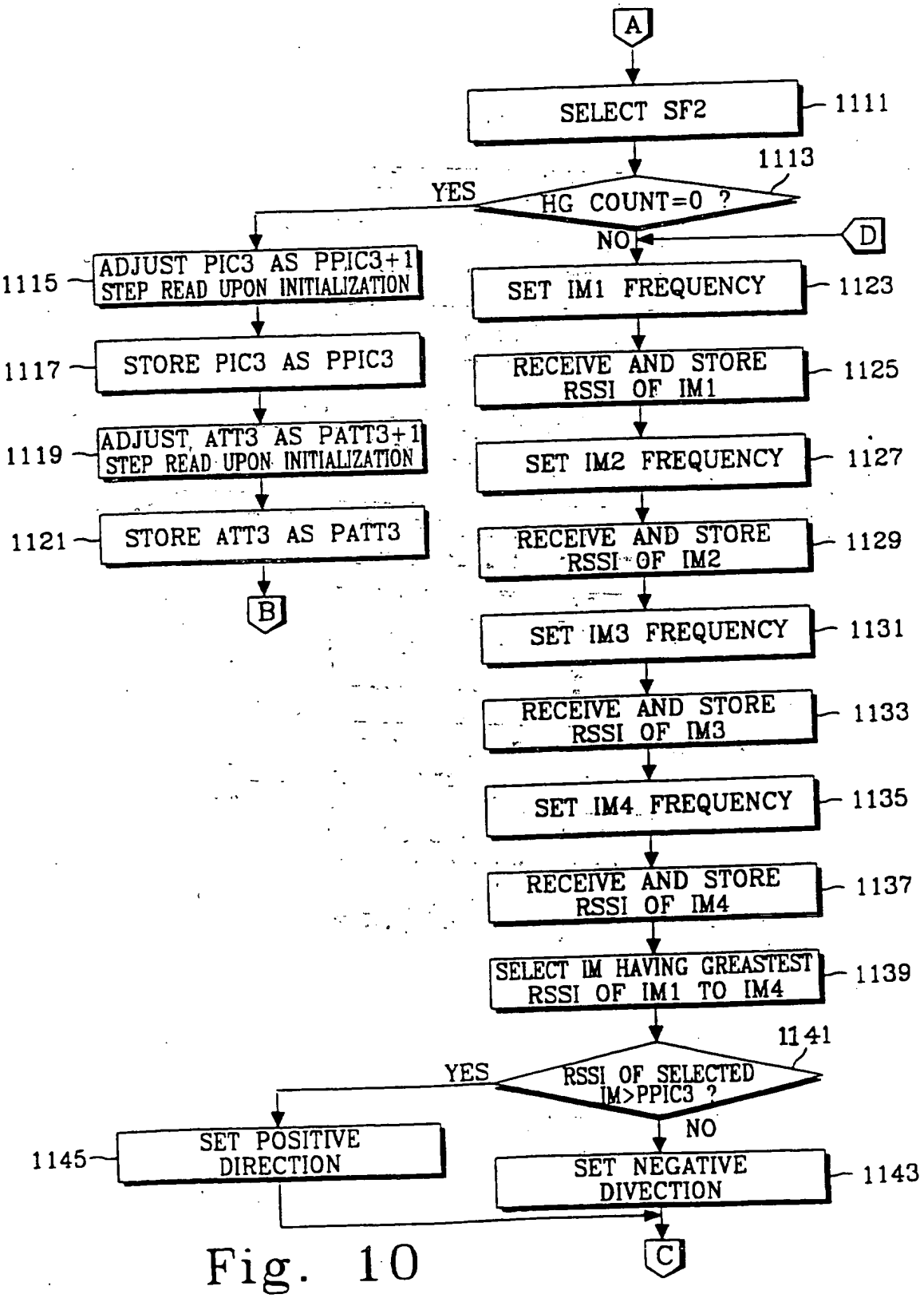

A
SELECT SF2
1111
1113
HG COUNT=0 ?
YES
NO
D
ADJUST PIC3 AS PPIC3+1 STEP READ UPON INITIALIZATION
1115
STORE PIC3 AS PPIC3
1117
ADJUST ATT3 AS PATT3+1 STEP READ UPON INITIALIZATION
1119
STORE ATT3 AS PATT3
1121
B
SET IM1 FREQUENCY
1123
RECEIVE AND STORE RSSI OF IM1
1125
SET IM2 FREQUENCY
1127
RECEIVE AND STORE RSSI OF IM2
1129
SET IM3 FREQUENCY
1131
RECEIVE AND STORE RSSI OF IM3
1133
SET IM4 FREQUENCY
1135
RECEIVE AND STORE RSSI OF IM4
1137
SELECT IM HAVING GREASTEST RSSI OF IM1 TO IM4
1139
1141
RSSI OF SELECTED IM>PPIC3 ?
YES
NO
SET POSITIVE DIRECTION
1145
SET NEGATIVE DIVECTION
1143
C

Fig. 10

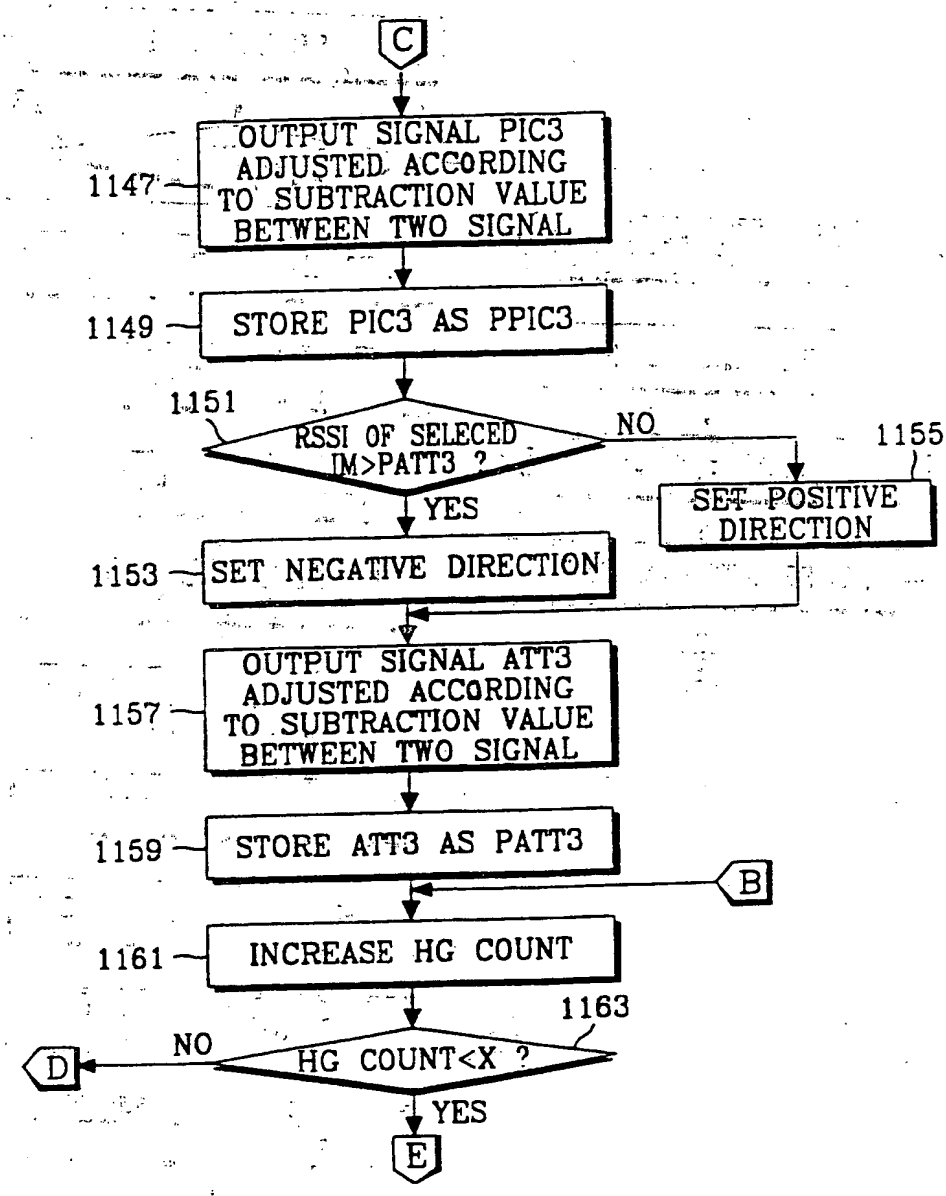

C
OUTPUT SIGNAL PIC3 ADJUSTED ACCORDING TO SUBTRACTION VALUE BETWEEN TWO SIGNAL
1147
STORE PIC3 AS PPIC3
1149
1151
RSSI OF SELECED IM>PATT3 ?
NO
1155
SET POSITIVE DIRECTION
YES
1153
SET NEGATIVE DIRECTION
OUTPUT SIGNAL ATT3 ADJUSTED ACCORDING TO SUBTRACTION VALUE BETWEEN TWO SIGNAL
1157
STORE ATT3 AS PATT3
1159
B
INCREASE HG COUNT
1161
1163
NO
HG COUNT<X ?
D
YES
E

Fig. 10

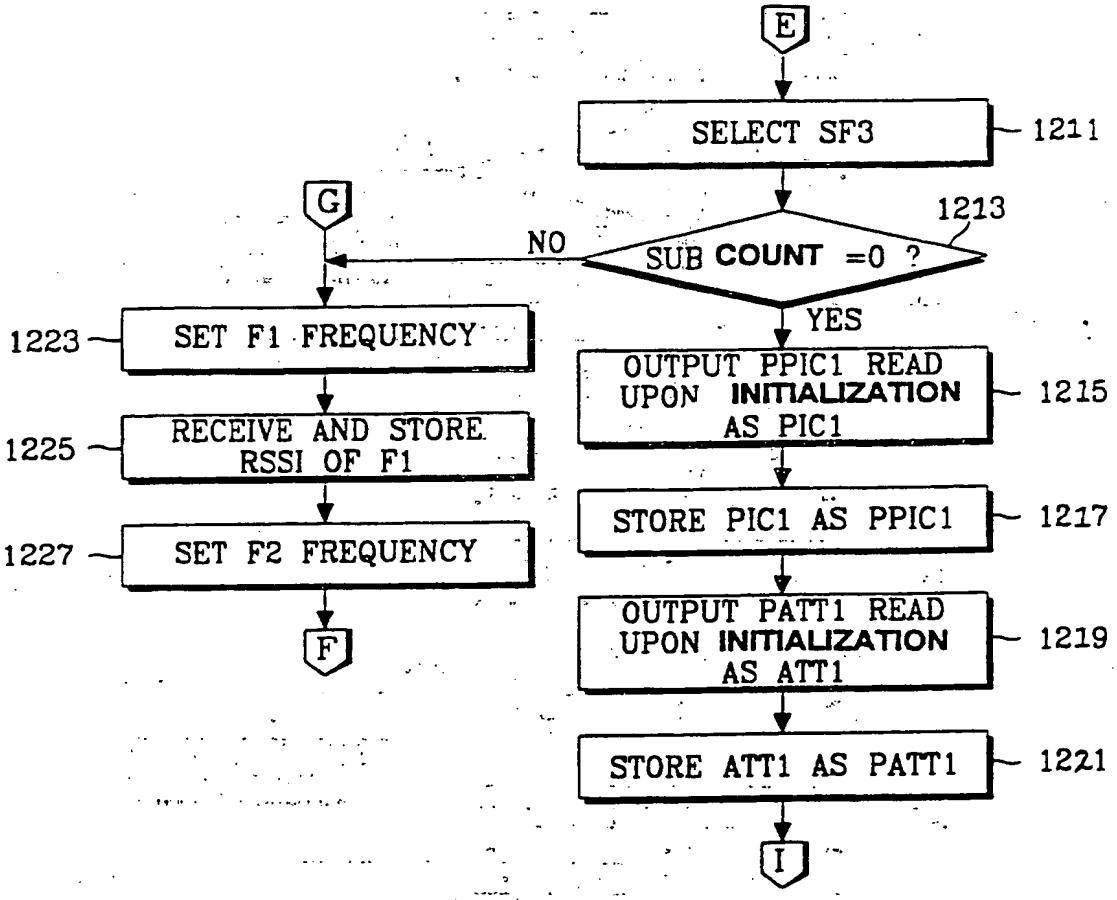
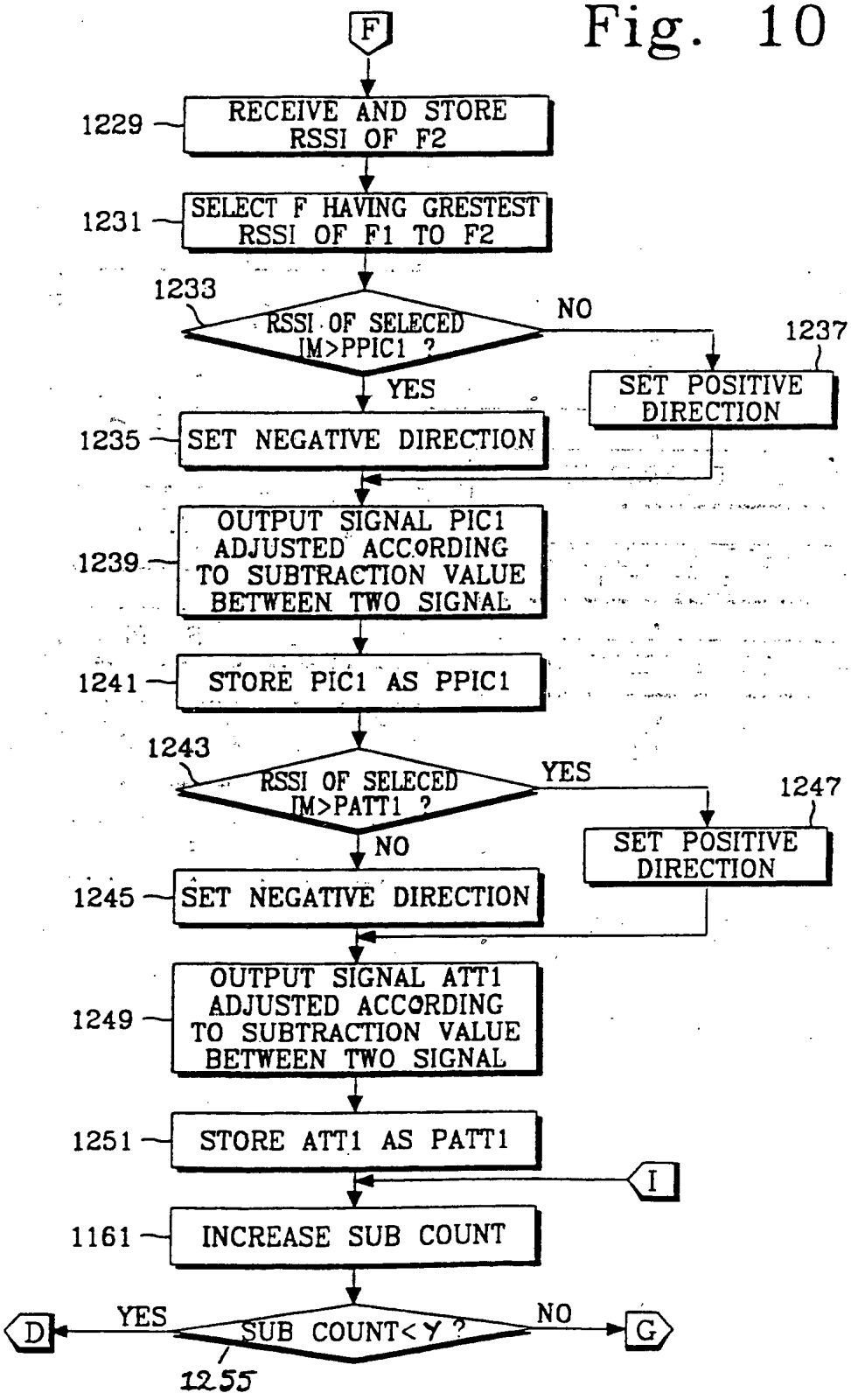

E
SELECT SF3
1211
1213
SUB COUNT =0 ?
NO
YES
G
1223
SET F1 FREQUENCY
1225
RECEIVE AND STORE RSSI OF F1
1227
SET F2 FREQUENCY
F
OUTPUT PPIC1 READ UPON INITIALIZATION AS PIC1
1215
STORE PIC1 AS PPIC1
1217
OUTPUT PATT1 READ UPON INITIALIZATION AS ATT1
1219
STORE ATT1 AS PATT1
1221
I

Fig. 10

Fig. 10


F
1229
RECEIVE AND STORE RSSI OF F2
1231
SELECT F HAVING GRESTEST RSSI OF F1 TO F2
1233
RSSI OF SELECED IM>PPIC1 ?
NO
1237
SET POSITIVE DIRECTION
YES
1235
SET NEGATIVE DIRECTION
1239
OUTPUT SIGNAL PIC1 ADJUSTED ACCORDING TO SUBTRACTION VALUE BETWEEN TWO SIGNAL
1241
STORE PIC1 AS PPIC1
1243
RSSI OF SELECED IM>PATT1 ?
YES
1247
SET POSITIVE DIRECTION
NO
1245
SET NEGATIVE DIRECTION
1249
OUTPUT SIGNAL ATT1 ADJUSTED ACCORDING TO SUBTRACTION VALUE BETWEEN TWO SIGNAL
1251
STORE ATT1 AS PATT1
I
1161
INCREASE SUB COUNT
D
YES
SUB COUNT<Y ?
NO
G
1255

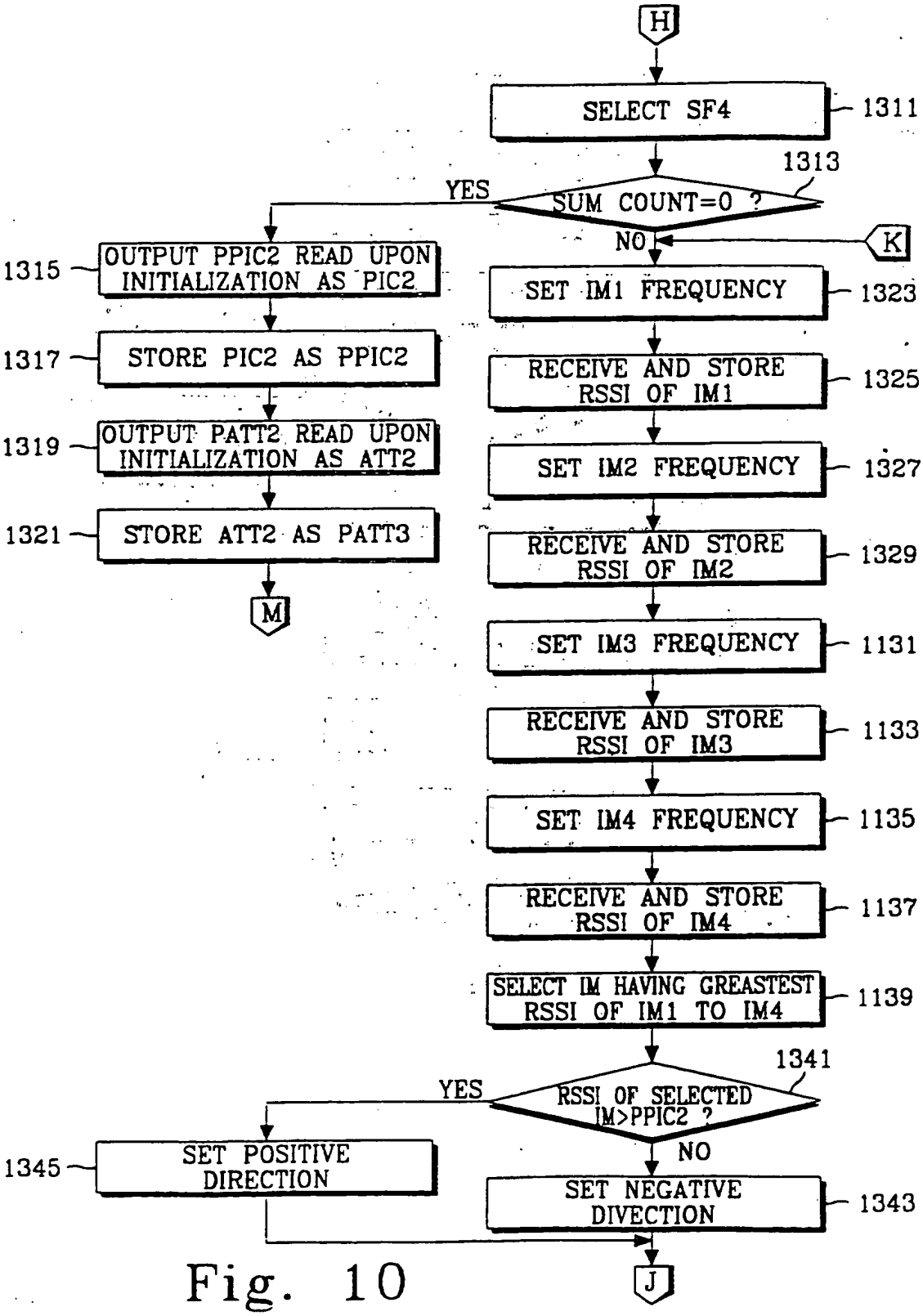

H
SELECT SF4
1311
1313
YES
SUM COUNT=0 ?
NO
K
1315
OUTPUT PPIC2 READ UPON INITIALIZATION AS PIC2
1317
STORE PIC2 AS PPIC2
1319
OUTPUT PATT2 READ UPON INITIALIZATION AS ATT2
1321
STORE ATT2 AS PATT3
M
SET IM1 FREQUENCY
1323
RECEIVE AND STORE RSSI OF IM1
1325
SET IM2 FREQUENCY
1327
RECEIVE AND STORE RSSI OF IM2
1329
SET IM3 FREQUENCY
1131
RECEIVE AND STORE RSSI OF IM3
1133
SET IM4 FREQUENCY
1135
RECEIVE AND STORE RSSI OF IM4
1137
SELECT IM HAVING GREASTEST RSSI OF IM1 TO IM4
1139
1341
YES
RSSI OF SELECTED IM>PPIC2 ?
NO
1345
SET POSITIVE DIRECTION
SET NEGATIVE DIVECTION
1343
J

Fig. 10

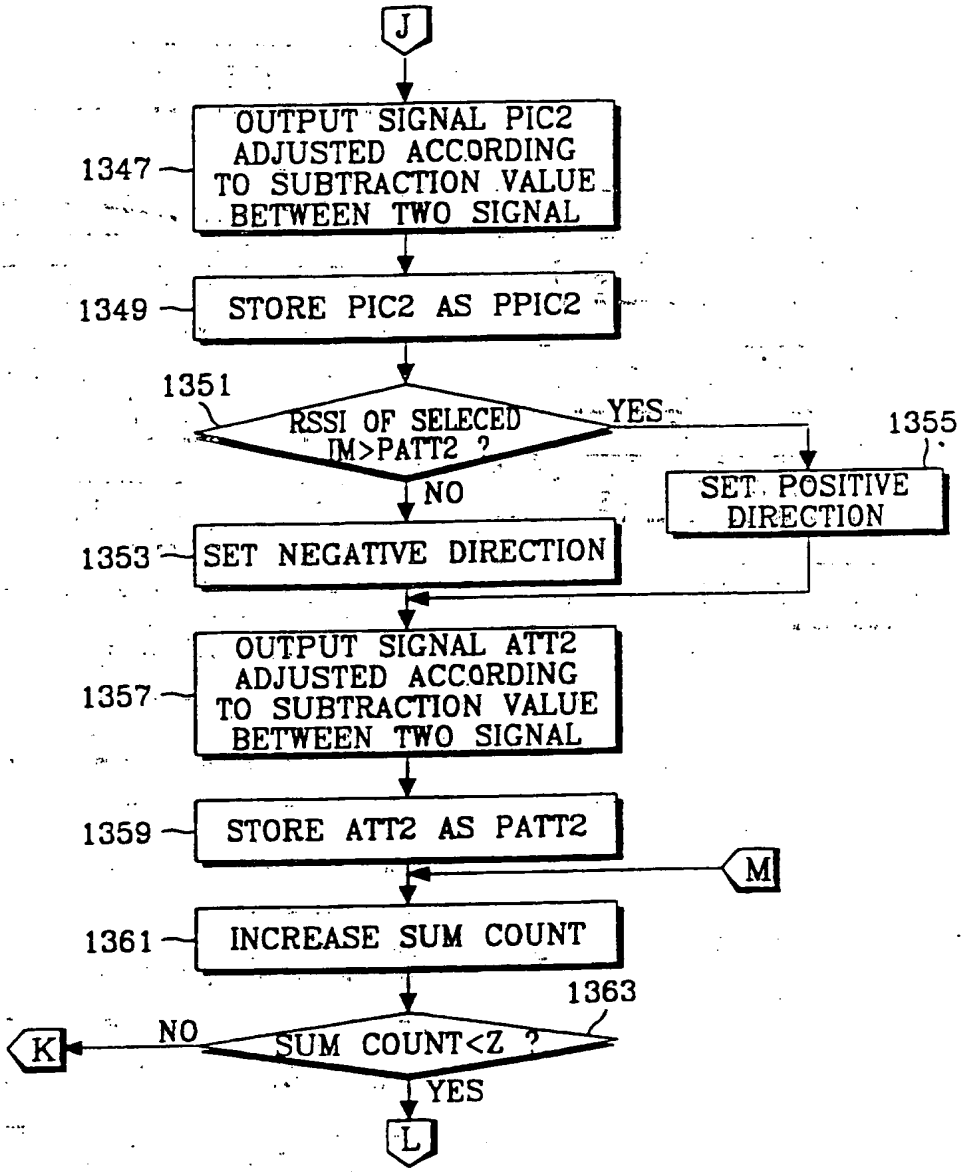

J
OUTPUT SIGNAL PIC2 ADJUSTED ACCORDING TO SUBTRACTION VALUE BETWEEN TWO SIGNAL
1347
STORE PIC2 AS PPIC2
1349
1351
RSSI OF SELECED IM>PATT2 ?
YES
NO
1355
SET POSITIVE DIRECTION
1353
SET NEGATIVE DIRECTION
OUTPUT SIGNAL ATT2 ADJUSTED ACCORDING TO SUBTRACTION VALUE BETWEEN TWO SIGNAL
1357
STORE ATT2 AS PATT2
1359
M
INCREASE SUM COUNT
1361
1363
SUM COUNT<Z ?
NO
K
YES
L

Fig. 10

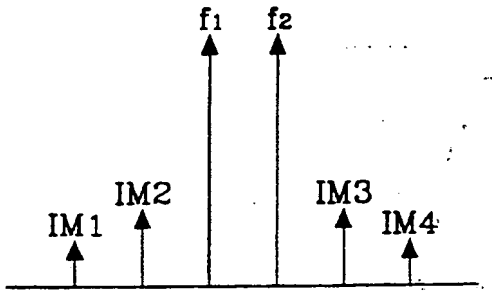


Fig. 11A

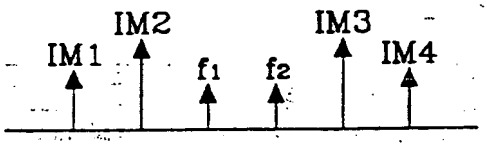


Fig. 11B

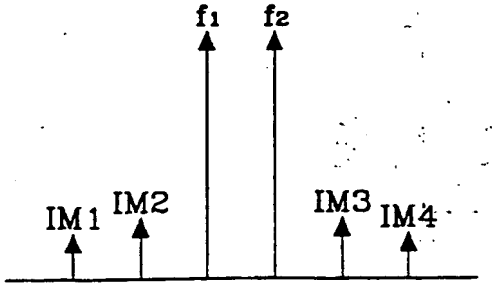


Fig. 11C

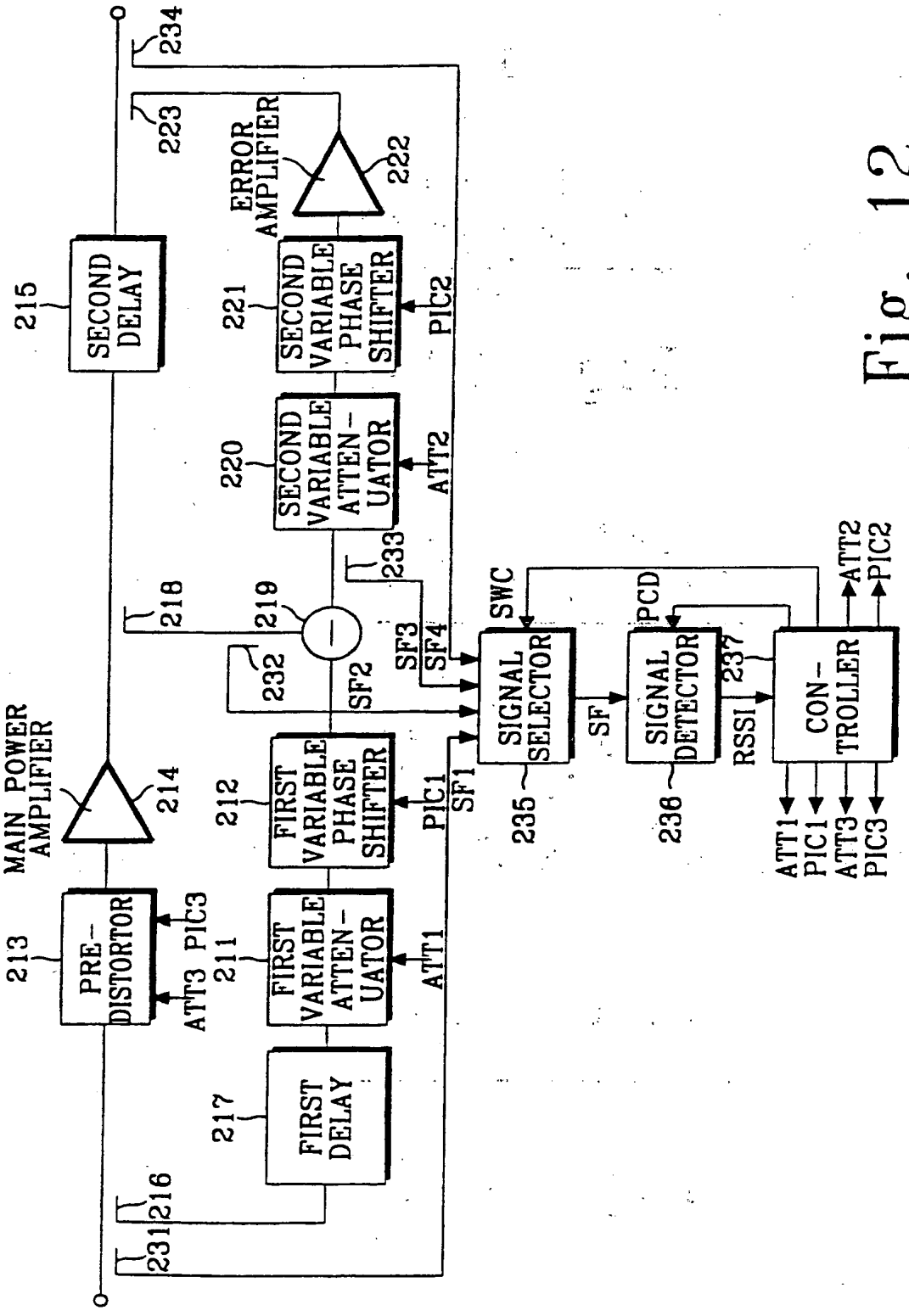

MAIN POWER AMPLIFIER
214
PRE-DISTORTOR
213
ATT3 PIC3
FIRST VARIABLE ATTEN-UATOR
211
ATT1
FIRST DELAY
217
216
231
FIRST VARIABLE PHASE SHIFTER
212
PIC1
SF1
232
218
219
SF2
SF3
SF4
233
SECOND VARIABLE ATTEN-UATOR
220
ATT2
SECOND VARIABLE PHASE SHIFTER
221
PIC2
SECOND DELAY
215
ERROR AMPLIFIER
222
223
234
SWC
SIGNAL SELECTOR
235
SF
PCD
SIGNAL DETECTOR
236
RSSI
237
CON-TROLLER
ATT1
PIC1
ATT3
PIC3
ATT2
PIC2

Fig. 12

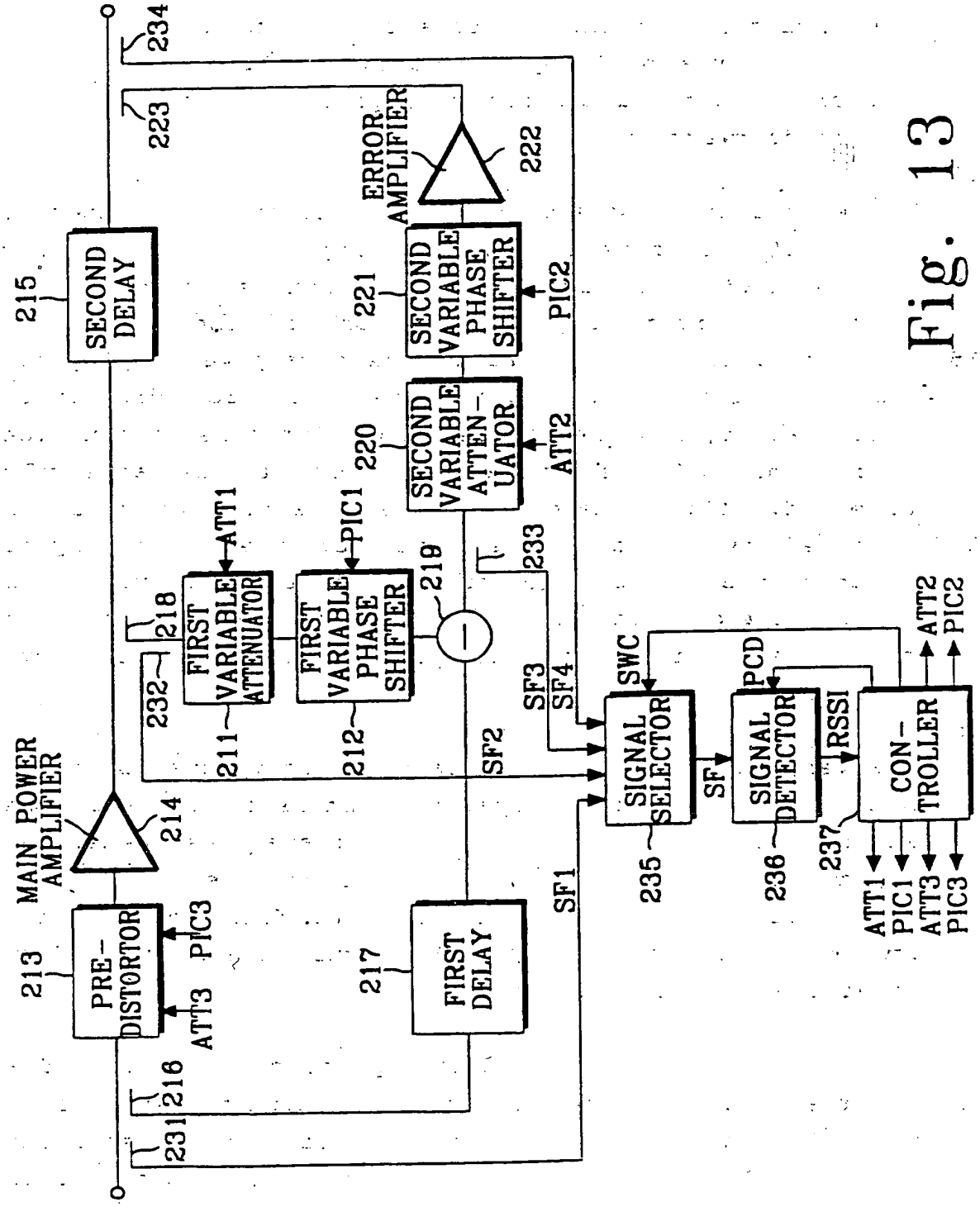

MAIN POWER AMPLIFIER
214
PRE-DISTORTOR
213
PIC3
ATT3
216
231
FIRST DELAY
217
SECOND DELAY
215
234
223
ERROR AMPLIFIER
222
SECOND VARIABLE PHASE SHIFTER
221
PIC2
SECOND VARIABLE ATTEN-UATOR
220
ATT2
233
218'
FIRST VARIABLE ATTENUATOR
218
ATT1
232
211
FIRST VARIABLE PHASE SHIFTER
PIC1
212
SF2
SF3
SF4
SWC
SIGNAL SELECTOR
235
SF1
SF
SIGNAL DETECTOR
236
PCD
RSSI
CON-TROLLER
237
ATT2
PIC2
ATT1
PIC1
ATT3
PIC3

Fig. 13

LINEAR POWER AMPLIFYING DEVICE AND METHOD

BACKGROUND OF THE INVENTION

The present invention relates to a linear power amplifying device and method and, more particularly, to linear power amplifying device and method for removing intermodulation distortion through predistortion system and feedforward system.

In general, high power amplifiers (hereinafter, referred to as HPA) operate in the vicinity of the saturation region having nonlinear characteristics in order to generate maximum output. However, in the case of a multi-carrier input signal to the high power amplifier, the multi-carrier generates intermodulation distortion (hereinafter, referred to as IMD). For this reason, the performance of the above amplifier can be adversely affected. Thus, there is generated a problem which is resolved by reducing the level of the input signal reduced by a number of dB or by using a power transistor having more capacity than a general transistor to prevent the deterioration in the performance of the above amplifier.

However, in this case, if a large capacity transistor is not used but a proper capacity transistor is used, the linear power amplifier can eliminate the generated intermodulation distortion by using the linearity. Therefore, the linear power amplifier necessarily improves the quality of an RF signal transmitted from communication apparatuses using such an amplifier.

FIG. 1 is a block diagram showing the construction of a prior art linear power amplifier, which is disclosed in the U.S. Patent No. 5, 130,663 granted to Tattersall and issued on July 14, 1992. Since the linear power

amplifier having the same construction as that of FIG. 1 generates a pilot signal, couples the generated signal to an input signal, detects the pilot signal in a final output terminal and controls the phase and the gain of an error amplifier, the intermodulation distortion can be suppressed accordingly. That is, the linear power amplifier utilizes the pilot signal so as to continuously suppress the phase and the gain of the error amplifier regardless of the variable operating conditions for the purpose of removing the intermodulation distortion.

But, now that the linear power amplifier using the pilot signal as illustrated in FIG. 1 operates without consideration of variation in operating conditions, it is difficult to set the condition for automatically adjusting the linear amplification with the above amplifier. Also, because the linear power amplifier additionally includes a pilot generator and a pilot detector etc., the construction and the control operation of the linear power amplifier may be complex.

As described above, a predistortion system for generating the predistortion in the input signal and improving the intermodulation suppression characteristics of the main amplifier, a negative feedback system for feeding back the distortion and suppressing the distortion included in the output of the amplifier, and a feedforward system for extracting only the distortion, making the back phase, and suppressing the extracted distortion are exemplary of linear power amplifying methods for eliminating the intermodulation distortion without using the pilot system.

SUMMARY OF THE INVENTION

Accordingly, the present invention provides a linear power amplifying device having a main power amplifier for eliminating an intermodulation signal, comprising:

a predistortor for firstly suppressing said intermodulation signal generated upon amplification of an RF signal in said main power amplifier, by generating a harmonics corresponding to said inputted RF signal and a predistortion signal with coupling said RF signal to said harmonics; and

a feedforwarder for secondly suppressing said intermodulation signal by cancelling said inputted RF signal and the output of said main power amplifier, extracting an intermodulation signal distortion, error-amplifying said extracted intermodulation signal distortion, and coupling said amplified intermodulation signal with the output of said main power amplifier.

An embodiment provides a linear power amplifying device having a main power amplifier, for eliminating an intermodulation signal, comprising: a predistortor for firstly suppressing the intermodulation signal generated upon amplification of an RF signal in the main power amplifier, by generating harmonics corresponding to the input RF signal and a predistortion signal for coupling the RF signal to the harmonics; and a feedforward arrangement for secondly suppressing the intermodulation signal by cancelling the input RF signal and the output of the main power amplifier, extracting an intermodulation signal distortion, error-amplifying the extracted intermodulation signal distortion, and coupling the amplified intermodulation signal with the output of the main power amplifier.

Further, the present invention also provides a method for eliminating an intermodulation signal of a linear power amplifying device which includes a main power amplifier, comprising the steps of: (a) firstly suppressing the intermodulation signal generated upon amplification of an RF signal in the main power amplifier, by generating harmonics corresponding to the input RF signal and a predistortion signal for coupling the RF signal to the harmonics; and (b) secondly suppressing the intermodulation signal by cancelling the input RF signal and the output of the main power amplifier, extracting an intermodulation signal distortion, error-amplifying the extracted intermodulation signal distortion, and coupling the amplified intermodulation signal with the output of the main power amplifier.

Advantageously, the present invention provides a linear power amplifying device and method for dividing and removing the intermodulation distortion with the predistortion system and the feedforward system.

Preferably, an embodiment of the present invention provides a linear power amplifying device and method for suppressing the intermodulation distortion generated in a main amplifier with the predistortion system and suppressing the intermodulation distortion included in an amplified signal finally outputted.

It is still another object of the present invention to provide linear power amplifying device and method, which installs a predistortor at a front terminal, beforehand expects the intermodulation distortion to be generated in the main amplifier, generates a predistortion signal, and inputs the generated predistortion signal to the main amplifier, thereby firstly suppressing the intermodulation distortion generated in the main amplifier.

It is further another object of the present invention to provide linear power amplifying device and method for extracting the rest of the intermodulation distortion included in the output of the main amplifier where the intermodulation distortion is first suppressed and coupling the extracted intermodulation distortion to finally-outputted signal, thereby secondly suppressing the intermodulation distortion in the amplifying signal finally outputted.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of this invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings, in which like reference symbols indicate the same or similar components, wherein:

FIG. 1 is a block diagram showing the construction of a prior art linear power amplifier;

FIG. 2 is a block diagram showing the construction of a linear power amplifier according to a first embodiment of the present invention;

FIG. 3 is a view showing the construction of a predistortor of FIG. 2;

FIG. 4 is a view showing the construction of an automatic level controller of FIG. 3;

FIG. 5 is a view showing the construction of a signal detector of FIG. 4;

FIGs. 6A to 6G are views showing the characteristic of the signal spectrum for explaining the operation of the

linear power amplifier according to a first embodiment of the present invention as shown in FIG. 2;

FIG. 7 is a view showing the construction of a signal detector of FIG. 2;

FIG. 8 is a view showing the construction of a controller of FIG. 2;

FIG. 9 is a flow chart showing the operation of attenuation and phase controlling functions of the controller according to an embodiment of the present invention;

FIG. 10 is a flow chart showing the operation of controlling a variable attenuator and a variable phase shifter of FIG. 2 by the controller according to an embodiment of the present invention;

FIGs. 11A to 11C show the signal spectrums for setting a frequency to control the attenuation and the phase of a signal in FIG. 10;

FIG. 12 is a block diagram showing the construction of a linear power amplifier according to a second embodiment of the present invention; and,

FIG. 13 is a block diagram showing the construction of a linear power amplifier according to a third embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following description, specific details such as components and frequencies of the circuits, are set forth to provide a more thorough understanding of the present invention. It will be apparent, however, to one skilled

in the art that the present invention may be practised without these specific details. The detailed description of known functions and constructions unnecessarily obscuring the subject matter of the present invention will be avoided in the present invention.

FIG. 2 is a block diagram showing the construction of a linear power amplifier according to a first embodiment of the present invention. With respect to FIG. 2, a first variable attenuator 211 controls the variation of the gain of the input RF signal using an attenuation control signal ATT1. A first variable phase shifter 212 receives the output of the first variable attenuator 211 and controls the phase of the input RF signal using a phase control signal PC11.

A predistortor 213 receives the RF signal, anticipates the harmonics of the intermodulation distortion expected to be generated in a main power amplifier 214 of a final terminal and generates an appropriate distortion signal. The main power amplifier 214 power amplifies the RF signal output from the predistortor 213 and outputs the power-amplified signal. A second delay unit 215 receives the power-amplified RF signal output by the main power amplifier 214, delays that signal and outputs the power-amplified RF signal during the time when the distortion signal is applied. The construction and signal processing as mentioned hereinbefore is considered as the main path of the linear power amplifier according to a preferred embodiment of the present invention.

A power divider 216 divides the input RF signal between the main path and a first delay unit 217. A suitable power divider would be a directional coupler. The first delay 217 compensates for the delay time of the RF signal in the predistortion and amplification process of the main path. A power divider 218 is positioned at an

output terminal of the main power amplifier 214 and divides the output of the main power amplifier 214. Like the power divider 216, a directional coupler can be used as the power divider 218. A signal canceller 219 receives the RF signal output by the first delay 217 and the amplified RF signal output by the power amplifier 214. The signal canceller 219 subtracts the RF signal output by the first delay 217 from the output of the main power amplifier 214, thereby detecting the intermodulation signal. In the embodiment of the present invention, the signal canceller 219 is embodied as the subtractor.

A second variable attenuator 220 receives the intermodulation signal output from the signal canceller 219 and controls the amplitude of the received intermodulation signal using an attenuation control signal ATT2 output from a controller 237. A second variable phase shifter 221 receives the intermodulation signal output by the second variable attenuator 220 and controls the phase of the input intermodulation signal using a phase control signal PIC2 output from the controller 237. An error amplifier 222 amplifies the intermodulation signal output from the second variable phase shifter 221 and outputs the amplified intermodulation signal. A signal coupler 223 couples the output of the error amplifier 222 to the output terminal of the second delay 215. Again, a directional coupler can be used as a suitable signal coupler 223.

The construction as stated above represents a sub-path for suppressing the intermodulation signal of the main path in the preferred embodiment of the present invention.

A power divider 231, positioned at the input terminal, also divides the input RF signal and outputs a first

signal SF1. A power divider 232 is disposed at the output terminal of the main power amplifier 214, divides the amplified RF signal and outputs a second signal SF2. A power divider 233, positioned at the output of the signal canceller 219, divides the intermodulation signal and outputs a third signal SF3. A power divider 234, provided at the output terminal, divides the final output RF signal, to produce a fourth signal SF4. The power dividers 231 to 234 can be realised with directional couplers. A signal selector 235 receives as inputs the above signals SF1 to SF4 and selectively outputs one of the input signals SF1 to SF4 as an output signal SF according to an input signal, switching control data SWC, output by the controller 237.

A signal detector 236 determines a received signal strength indicator (hereinafter, referred to as RSSI) of the signal SF output by the signal selector 235 according to control data PCD (PLL control data) which is output by the controller 237 and then outputs an RSSI signal which is converted into the direct current. The controller 237 generates the switching control signal SWC for selection of the signal SF pertaining to the signal selector 235 and thus, the control data PCD for determining the frequency for detection of the RSSI of the signal SF selected by the signal detector 236.

Additionally, the controller 237 analyzes the value of the RSSI signal output by the signal detector 236 and generates the attenuation control signals ATT1 to ATT3 and the phase control signals PIC1 to PIC3, the above signals controlling the variable attenuator and the variable phase shift in order to adjust the gain and the phase of the signal SF according to the result of the analysis controller 237. In the case where the input signal output by the power divider 231 is selected, that is signal SF1, the controller 237 controls the signal

detector 236, detects the RSSIs of the input RF signal, and determines the size of the RSSIs, so that the frequency component of the input RF signal can be recognized, accordingly. In the case where the output of the main power amplifier 214 output by the power divider 232 is selected, that is signal SF2, the controller 237 controls the signal detector 236, detects the RSSIs of the harmonics signal of the amplified RF signal, and determines the size of the RSSIs, thereby generating an attenuation control signal ATT3 and a phase control signal PIC3, each signal for adjusting the attenuation and the phase of the intermodulation signal output by the predistortor 213. Secondly, when the output of the signal canceller 219 is selected, that is signal SF3, the controller 237 controls the signal detector 236, detects the RSSIs of the RF signal contained in the cancelled intermodulation signal, and judges the size of the RSSIs, thereby generating the attenuation control signal ATT1 and the phase control signal PIC1, each signal for adjusting the attenuation and the phase of the RF signal input to the input terminal of the linear power amplifier. Thirdly, when the amplified signal which is finally output is selected, that is signal SF4, the controller 237 controls the signal detector 236, detects the RSSIs of the intermodulation signals included in the signal finally output, and determines the size of the RSSIs, thereby generating the attenuation control signal ATT2 and the phase control signal PIC2, each signal for adjusting the attenuation and the phase of the intermodulation signal output by the signal canceller 219.

According to a preferred embodiment of the present invention as constructed above, the linear power amplifier eliminates the intermodulation signal which can occur in the amplification step by using the predistortion system and the feedforward system. In the

above embodiment of the present invention, the predistortor 213 firstly performs the function of removing the intermodulation signal which is output by the main power amplifier 214. In order to realise the above operation, the predistortor 213 anticipates the harmonics which can be expected to be generated upon amplification of the RF signal by the main power amplifier 214 and to then adjust the phase of the RF signal so as to have the back phase with the harmonics capable of being generated in the main power amplifier 214, to thereby be outputted, at the time when the harmonics is applied to the power transistor of the main power amplifier 214.

As a consequence of using the predistortion system above, it is impossible to completely eliminate the intermodulation signal caused in the linear power amplifier. As a result, the linear power amplifier according to the embodiment of the present invention, firstly suppresses the intermodulation signal using the predistortor 213, and finally suppresses the intermodulation signal using an adaptive feedforward system. The linear power amplifier using the feedforward system, cancels pure RF signal distortion in the output of the main power amplifier 214, extracts the intermodulation signal, and couples the extracted intermodulation signal to the signal coupler 223, thereby cancelling the intermodulation distortion. Therefore, when using the feedforward system, the intermodulation signal distortion contained in the amplified signal output by the output terminal of the linear power amplifier can be suppressed, so that the pure amplified RF signal can be output.

In the embodiment of the present invention as explained above, the intermodulation signal generated in the amplification of the main power amplifier 214 is firstly

suppressed with using the predistortion system, and the intermodulation signal pertaining to the output of the main power amplifier 214 is secondly suppressed using the feedforward system. Herein, for the convenience of explanation, after the operation for suppressing the intermodulation signal by the predistortion system, it is intended that the operation for suppressing the intermodulation signal by the feedforward system may follow.

FIGs. 6A to 6G are views showing the characteristic of a signal spectrum for explaining the operation of the linear power amplifier according to the first embodiment of the present invention as depicted in FIG. 2. In FIGs. 6A to 6G two frequencies are used to demonstrate the operation of the embodiment shown in FIG 2. FIG. 6A shows the input signal RF. FIG. 6B shows the harmonics signal to the RF signal generated in a harmonic generator 314. FIG. 6C shows the spectrum of a signal which can adjust the size of the harmonics by a variable attenuator 315 in the predistortor 213 and have the adjusted phase capable of being input in anti-phase to the main power amplifier 214 by means of a variable phase shift 316. FIG. 6D shows the amplified RF signal containing the intermodulation signal produced by amplifying the predistortion signal input to the main power amplifier 214 as shown in FIG. 6C. Also, FIG. 6E shows the intermodulation signal extracted by cancelling the amplified RF signal using the signal canceller 219 as shown in FIG. 6A. FIG. 6F depicts the signal which adjusts the size of the intermodulation signal as shown in FIG. 6E and is in anti-phase with the output of the main power amplifier 215 as shown in 6D. FIG. 6G shows the final output signal from the linear power amplifier having suppressed the intermodulation signal by coupling the intermodulation signal extracted as shown in FIG. 6D

and the RF signal amplified as shown in FIG. 6D, to each other in anti-phase.

FIG. 3 is a view showing the construction of the predistortor 213 of FIG. 2. With reference to FIG. 3, the power divider 312 divides the RF signal positioned in the input terminal and outputs the divided RF signal to an automatic level controller (hereinafter, referred to as ALC). The ALC constantly maintains the level of the input RF signal in order to generate harmonics of a constant level regardless of the variation in the level of the input RF signal. The harmonics generator 314 receives the level adjusted RF signal from the automatic level controller 313 and generates third, fifth, seventh, and higher harmonics of the RF signal. A variable attenuator 315 receives the harmonics signal output by the harmonics generator 314 and controls the amplitude of the harmonics signal in response to the attenuation control signal ATT3 output by the controller 237. The variable phase shifter 316 receives and adjusts the phase of the harmonics signal output by the variable attenuator 315 according to the phase control signal PIC3 output by the controller 237. A second delay 311 delays the main path input RF signal during the period of time when the predistortion signal occurs. A signal coupler 317 is positioned between the output terminal of the second delay 311 and the input terminal of the main power amplifier 214, thereby coupling the predistortion signal to the delayed RF signal.

Referring to FIG. 3, the harmonics generator 314 is constructed with a signal coupler and a Schottkey diode. Then, upon input of the RF signal to the Schottkey diode, the Schottkey diode generates the high harmonics in accordance with the level of the input RF signal. Consequently, the level of the RF signal input to the Schottkey diode should be set to a level which is capable

of most effectively suppressing the intermodulation signal included in the output of the main power amplifier 214. To meet this requirement, the automatic level controller 313 is positioned before the harmonics generator 314 so that the RF signal can always be input at the appropriate level to the harmonics generator 314.

The automatic level controller 313 controls and outputs an RF signal of the desired level set regardless of the variation in the level of the RF signal input to the linear power amplifier. FIG. 4 is a view showing the construction of the automatic level controller 313 of FIG. 3, where a variable attenuator 412 is connected between the power divider 312 and the harmonics generator 314. A power divider 414 is disposed at the input terminal of the harmonics generator 314. The power divider 414 divides the outputs, the RF signal having an adjusted level between the harmonic generator 314 and a power detector 416. The power detector 415 converts the RF signal into a DC voltage and outputs the converted signal to a level controller 416. The level controller 416 controls the variable attenuator 412 according to the DC voltage output by the power detector 415, so that the RF signal maintains a desired level. Hence, a signal having a constant level can always be input to the harmonics generator 314.

The power detector 415 of FIG. 4 should be capable of handling a multi-carrier RF signal. Namely, the power detector 415 should receive the multi-carrier RF signal and convert the input RF signal into a corresponding DC voltage. FIG. 5 shows the construction of the power detector 415 of FIG. 4. An RF transformer 451 receives the RF signal and generates two signals having a relative phase difference of 180°. The two signals output from the RF transformer 451 are converted via transmission lines 452 and 453 and Schottkey diodes 454 and 455 into

a DC voltage level. The DC voltage level is then filtered via a capacitor 456 and a resistor 457. The filtered DC voltage signal is then output as a DC voltage.

With reference to FIGs. 3 and 4, regarding the operation for controlling the level of the input RF signal, the RF transformer 451 for generating the signals having a relative phase difference of 180°, generates two signals by separating the input RF signal by a unit of a semi-diameter. Further, the Schottkey diodes 454 and 455 convert the two signals input via the transmission lines 452 and 453 into the DC level, respectively. Accordingly, the average power of the multi-carrier can be determined without error, so that the level of the RF signal input to the harmonics generator 314 can accurately be converted into the DC voltage.

The level controller 416 generates the control signal according to the level of the DC voltage of the RF signal output from the power detector 415 and applies the generated control signal to the variable attenuator 412. The level controller 416 can be embodied using an operational amplifier. The control signal output from the level controller 416 is generated to vary the attenuation control. The attenuation is increased if the DC voltage of the detected RF signal increases. The attenuation is decreased if the DC voltage of the detected RF signal is decreased. Thus, the variable attenuator 412 variably attenuates the RF signal to a predeterminable level regardless of the level of the input RF signal and outputs the variably attenuated signal to the harmonics generator 314.

When the variation in the level of the input RF signal is 10dB, the operation of the automatic level controller 313 should be designed to control maintain its level above

the 10dB level, minimumly. In addition, the output level of the RF signal of the automatic level controller 313 should be set to suppress optimally the intermodulation signal which the harmonic generator 314 generates as an input to the main power amplifier 214 (as the predistortion signal). Therefore, since the harmonic generator 314 receives from the automatic level controller 313, an RF signal of a predetermined level, harmonics having a stable output level can be realised. Further, as the harmonics output by the harmonics generator 314 are input to the main power amplifier 214 coupled with the RF signal, the main power amplifier 214 can prevent the generation of the intermodulation signal during amplification of the RF signal.

Likewise, upon inputting the harmonics generated as above, the main power amplifier 214, the size and phase of the harmonics capable of being generated during amplification can be adjusted. The variable attenuator 315 and the variable phase shifter 316 as shown in FIG. 3, adjust the size of the harmonics generated according to size and phase of the intermodulation signal capable of being generated during amplification.

The controller 237 controls the signal selector 235 and selects the output of the main power amplifier 214 via the power divider 232. The signal detector 236 detects the RSSI of the intermodulation signal in the output of the main power amplifier 214 as shown in FIG. 6D. After comparing and analyzing the RSSI value of the intermodulation signal output by the signal detector 236 with the previous RSSI value, the attenuation control signal ATT3 and the phase control signal PIC3 are generated so as to smoothly control the suppression of the intermodulation signal generated by the main power amplifier 214.

The variable attenuator 315 adjusts the size of the predistortion signal generated in the harmonics generator 314 according to the attenuation control signal ATT3, and the variable phase shifter 316 adjusts the phase so that the predistortion signal can be input in anti-phase to the main power amplifier 214. As adjusted above, the size and phase of the harmonics signal as shown in FIG. 6D, which is generated in the harmonics generator 314 is adjusted and the signal coupler 317 couples the harmonics signal to the input terminal of the main power amplifier 214. As shown in FIG. 3, the second delay 311 delays the RF signal until the predistortion signal is coupled appropriately to the input terminal of the main power amplifier 214. Thereafter, it will be understood that the predistortion signal, comprising the RF signal and the harmonics signal, is coupled to the input terminal of the main power amplifier 214. Here, it is preferable to use the position where the intermodulation signal coupled to the RF signal as shown in FIG. 6C is adjusted with the back phase, as the input terminal of the power transistor of the main power amplifier 214.

As noted above, the predistortor 213 anticipates the intermodulation signal generated by the main power amplifier 214 to thereby generate the predistortion signal, and controls the phase and attenuation of the harmonics signal to prevent the intermodulation signal from being generated at a maximum value. In this event, the predistortor 213 mainly eliminates the third harmonics which typically have the highest level among those harmonics capable of being generated in the main power amplifier 214. The intermodulation signal elimination effect of the predistortion system can greatly reduce the levels of intermodulation signals by adapting the feedforward system. The predistortion system advantageously realises an improvement of the

order of several dB in the reduction of the intermodulation products.

After suppressing the intermodulation signal which is generated in the main power amplifier 214 using the predistortion system as mentioned previously, the remaining intermodulation signal which cannot be suppressed using the predistortion system is suppressed using the feedforward system. In the above feedforward system, the steps for reducing the intermodulation signal of the main power amplifier 214 are largely divided into two steps. The first step extracts the pure intermodulation signal distortion by subtracting the input RF signal from the output of the main power amplifier 214. The second step cancels the intermodulation signal distortion in the output of the main power amplifier 214 after correcting the size and the phase of the extracted intermodulation signal, so as to reduce the intermodulation signal included in the signal which is finally output by the linear power amplifier.

The explanation of the first step of the feedforward system will be given hereinafter. The power divider 216 on the sub-path divides the input RF signal (as shown in FIG. 6A) between the main path and the sub-path. The first delay unit 217 delays the divided RF signal during the period of the predistortion and RF amplification and then applies the delayed divided RF signal to the signal canceller 219. Thus, the RF signal, as shown in FIG. 6A, which is output from the first delay 217 is reciprocally cancelled with the amplified RF signal as shown in FIG 6D via a power divider 218, so as to extract and output the only intermodulation signal.

The signal canceller 219 detects only the intermodulation signal distortion introduced by the main power amplifier

214. The signal canceller 219 can be constructed as a subtractor or an adder. In the case of constructing the signal canceller 219 as a subtractor, the two RF signals to be input should be adjusted to be in phase. Also, in the case of constructing the signal canceller 219 as the adder, the two RF signals to be input should be adjusted to be in anti-phase relative to one another. Preferably, the signal canceller 219 is embodied not as a subtractor, but as an adder. In this case, the subtractor comprises a signal coupler for receiving one signal of two RF signals having the same phase as the other RF signal, and converts the other RF signal to be in anti-phase said one signal and thereby inputs the converted signal to the signal coupler. When the RF signal as illustrated in FIG. 6A and the amplified RF signal as illustrated in FIG. 6D are input to a signal canceller 219 embodied as a subtractor, the two RF distortion signals are in phase and are adjusted so that they are in anti-phase with each other in an interior thereof. Thereafter, the RF signal is cancelled while passing the signal coupler (herein, the Wilkinson combiner can be used), thereby extracting only the intermodulation signal distortion.

At this point, each of levels and phases of two RF signals input to the signal canceller 219 should be exactly equal to each other. In order to meet this requirement, the amplified RF signal output by the main power amplifier 214 of the main path and the RF signal to be input via the sub-path should be precisely accorded with the group delay as well as the characteristic of the flatness of the delay being positive. That is, it is preferable that the phase distortion of the RF signal desired to be cancelled should be prevented from being generated to the greatest extent possible.

As described above, when the level and the phase of the RF signal output by the first delay 217 and the output of

the main power amplifier 214 are not exactly in phase with each other, the RF signal is not precisely cancelled by the signal canceller 219. To alleviate the above, the first variable attenuator 211 of FIG. 2 adjusts the level of the input RF signal according to the attenuation control signal ATT1 output by the controller 237 and the first variable phase shifter 212 adjusts the phase of the input RF signal according to the phase control signal PIC1 which is output by the controller 237. Accordingly, the first variable attenuator 211 and the first variable phase shifter 212 respectively, adjusts the phase and the level of the RF signal of the sub-path to bring them into agreement with phase and level of the RF signal of the main path. Thus, the signal canceller 219 cancels two input RF signals having the same level and phase with each other.

As mentioned previously, in order to control the phases and the levels of two RF signals, the controller 237 outputs the switch control signal SWC for selection of a third signal SF3, to the signal selector 235 and outputs the control data PCD for detection of the RSSI of the RF signal distortion of the third signal SF3 in the signal detector 236. As a consequence, the signal selector 235 selectively receives the third signal SF3, that is the output of the signal canceller 219, via the power divider 233, and the signal detector 236 generates the corresponding RSSI which converts the RF signal distortion of the third signal SF3 into a DC voltage. The controller 237 then generates the attenuation control signal ATT1 and the phase control signal PIC1 for attenuation of the RF signal distortion in the signal canceller 219.

The first variable attenuator 211 attenuates the input RF signal by determining the attenuation ratio according to way of the attenuation control signal ATT1, and the first

phase variable phase shifter 212 adjusts the phase of the input RF signal according to the phase control signal PIC1. Since the attenuation control signal ATT1 and the phase control signal PIC1 are generated after comparing and analyzing, firstly, the RSSI of the RF signal to be output in the signal canceller 219 and, secondly, the RSSI of the previous RSSI with each other, the first variable attenuator 211 and the first variable phase shifter 212 controls two RF signals as shown in FIGs. 6D and 6A so that they have the same phases and the levels relative to one another.

The reason for cancelling the RF signal distortion in the signal canceller 219 as stated before, is to have no influence on the error amplifier 222 positioned at the output terminal by greatly suppressing the RF signal and solely extracting the intermodulation signal distortion. Namely, if the output of the signal canceller 219 is changed and the RF signal is not effectively eliminated, the RF signal having a relatively large level is input to the error amplifier 222, thereby having an adverse effect on the operation of the error amplifier 222.

Secondly, the explanation of the second step of the feedforward system will be given hereinafter. The intermodulation signal output by the signal canceller 219 as above adjusts its phase and level through the second variable attenuator 220, the second variable phase shifter 221, and the error amplifier 222, and the intermodulation signal distortion included in the output of the main power amplifier is removed by inputting the adjusted signal to the main path. At this time, the intermodulation signal coupled by a signal coupler 223 should be in anti-phase with the amplified and output signal.

Here, the controller 237 generates the switch control signal SWC for selecting the fourth signal SF4. The fourth signal SF4 is derived, via a power divider 234, from the final output of the linear amplifier. The controller 237 outputs the control data PCD for detection of the RSSI of the harmonics of the intermodulation signal of the fourth signal SF4. Thus, the signal selector 235 selectively outputs the fourth signal SF4 according to the switch control signal SWC and the output of the signal detector 236 is applied to the controller 237 which detects the RSSI of the harmonics of the fourth signal SF4 according to the control data PCD. The controller 237 then compares and analyses the RSSI of the intermodulation signal included in the output signal of the linear amplifier with the RSSI of the previous intermodulation signal, so that the attenuation control signal ATT2 and the phase control signal PIC2 for suppression of the intermodulation signal included in the output signal of the linear amplifier can be generated according to the result of the comparison and analysis.

Therefore, the second variable attenuator 220 receiving the output of the signal canceller 219 adjusts the level of the input intermodulation signal according to the attenuation control signal ATT2, and the degree of the phase shift of second variable phase shifter 221 which receives the signal output from the second variable attenuator 220 adjust the phase of the intermodulation signal according to the phase control signal PIC2. The second variable phase shifter 221 controls the phase of the intermodulation signal so that it is in anti-phase with the signal derived from the signal coupler 223 by means of the phase control signal PIC2. Thus, the error amplifier 222 connected between the second variable phase shifter 221 and the signal coupler 223 amplifies and outputs the intermodulation signal having a level and phase adjusted as above.

As discussed above, the linear power amplifier according to the above embodiment of the present invention, uses the feedforward system and the predistortion system in order to suppress the intermodulation signal which typically results from or amplification of a signal. In order to suppress the intermodulation signal, the intermodulation signal capable of being generated in the main power amplifier 214 is anticipated and suppressed by the predistortion system and the intermodulation signal included in the output of the main power amplifier 214 is detected by the feedforward system, coupled to the output of the linear amplifier which thereby reduces the intermodulation signal in a sequential manner. As it is difficult to design and construct the main power amplifier 214 and the error amplifier 222, the intermodulation signal of a given size is only suppressed to a certain degree, but not wholly, by using the predistortor 213 and the remaining intermodulation signals are eliminated by the feedforward system. This enables the design and construction of the linear power amplifier to be realised.

Next, the steps of suppressing the intermodulation signal by using the feedforward system and the predistortion system centring on the controller 237 will be described in the following description.

FIG. 7 is a view showing the construction of the signal detector 236 of FIG 2 according to the present invention.

Referring to FIG. 7, an attenuator 711 attenuates and outputs an SF signal received from the signal selector 235. A wideband filter 712 filters the signal of the transmitting band. A phase lock loop (hereinafter, referred to as PLL) 713 and an oscillator 714 generate a corresponding local frequency LF1 according to the control data PCD output from the controller 237. The

above local frequency LF1 is used to determine the frequency for detecting the RSSI of the selected SF signal. A mixer 715 mixes the signal output from the filter 712 with the local frequency LF1 and thus generates an intermediate frequency IF. An intermediate frequency filter 716 filters a subtraction signal, representing the subtraction, SF-LF1, of two frequencies, output by the mixer 715, thereby generating the filtered intermediate, IF1, signal from a local frequency LF1. An oscillator 719 generates a fixed local frequency LF2. The mixer 718 mixes the intermediate frequency IF1 output from an intermediate frequency amplifier 717 and the fixed local frequency LF2 to generate an intermediate frequency IF2. A filter 720 filters a subtraction signal, IF1-LF2, of two frequencies output from the mixer 718 and outputs the filtered intermediate signal IF2. A log amplifier 712 converts the intermediate frequency IF2 output from the filter 720 into a DC voltage and generates from the converted voltage RSSI signal.

When observing the operation of FIG. 7, the signal selector 235 selectively outputs the corresponding RF signal selected from the first signal SF1 to the fourth signal SF4 according to the switch control signal SWC of the controller 237. Thus, the filter 712 of the signal detector 236 filters the RF signal and applies the filtered RF signal to the mixer 715. And then, the PLL 713 and the oscillator 714 generate the local frequency LF1 for selection of the RF signal or the harmonics of the signal selected according to the control data PCD of the controller 237. Consequently, the mixer 715 mixedly outputs the SF signals and the local frequency LF1 and the filter 716 filters the frequency corresponding to the subtraction between two signals and outputs the filtered frequency as the intermediate frequency IF1. The construction as described above determines the frequency for detection of the RSSI in the selected SF signal and

performs the frequency down conversion of the first step, at the same time.

Hereinafter, the mixer 718 mixes the local frequency LF2 and the intermediate frequency IF1 output from the oscillator 719 and the filter 720 filters the frequency corresponding to the subtraction or difference between the intermediate frequency IF1 and the local frequency LF2 of the mixed signals, thereby outputting the filtered frequency as the intermediate frequency IF2. The frequency down conversion of the second step is performed via the above construction. The logic amplifier 721 receives the intermediate frequency IF2 and converts the intermediate frequency IF2 into a DC voltage to be output. The output signal represents the RSSI.

FIG. 8 is a view showing the construction of the controller 237 of FIG. 2. In FIG. 8, an analog to digital converter 814 (hereinafter, referred to as ADC) converts the RSSI output from the signal selector 236 into digital data. A read only memory 812 (hereinafter, referred to as ROM) stores a program for controlling the attenuation and the phase in accordance with an embodiment of the present invention. A central processing unit 811 (hereinafter, referred to as CPU) generates the control data PCD for selection of the frequency of LO714 required to select the selected SF signal for which a determination has to be made of the corresponding RSSI. The CPU 811 also generates the switch control signal SWC for selection of the RF signal depending on the program of the ROM 812, and generates the attenuation control signals ATT and the phase control signals PIC after comparing and analyzing the RSSI output from the ADC 814 with each other. A random access memory 813 (hereinafter, referred to as RAM) temporarily stores all kinds of data which are generated in the process of performing the program. A digital to analog converter

815 (hereinafter, referred to as DAC) converts the attenuation control data and the phase control data output from the CPU 811 into analog signals and outputs the converted data as the attenuation control signals ATT and the phase control signals PIC. A communicator 816 outputs information relating to the state of the linear power amplifier under the control of the CPU 811.

FIG. 9 is a flow chart showing the operation of adjusting the attenuation level and the phase by controlling the above variable attenuators and the variable phase shifters according to the outputs of the controller 237 according to an embodiment of the present invention.

As shown in FIG. 9, the "X" axis indicates attenuation values and the "Y" axis indicates phase variation values. With reference to FIG. 9, upon changing the value of the variable attenuator from Pa to Pb at the point when the RSSI is input, if the size of the detected signal is decreased, the phase variation value is changed from Pb to Pc. After that, in the event that the value of the variable attenuator is changed from Pc to Pd at the point when the RSSI is input, if the detected signal is again increased, the phase variation value is changed in the direction of Pc. Herein, Pc is indicated as the point where the size of the attenuation value is temporary. Accordingly, the phase variation value is changed from Pc to Pe and the size of the detected RSSI is decreased, the variable phase shifter moves the phase variation value in the direction of Pf.

When attenuation and phase operations are repeatedly controlled as stated above, there can be found values of the variable attenuator and the variable phase shifter for which the size of the detected SF signal is minimized. FIG. 10 is a flow chart showing the operations of the variable attenuator and the variable

phase shifter of the controller 237 according to an embodiment of the present invention. As set forth in FIG. 10, after firstly controlling the phase of the detected signal, the function of attenuating the signal is performed. However, it is possible to control the phase of the signal after attenuation of the signal.

Referring to FIG. 10, eliminating intermodulation distortion is largely divided into 4 stages. Firstly, the RSSI of the first signal SF1 is detected, a channel where the RF signal is detected in the transmitting band is set, thereby determining service channels. Secondly, the RSSI of the second signal SF2 is detected and the main power amplifier 214 suppresses the intermodulation signal to amplify the received RF signal, thereby generating the predistortion signal. Thirdly, the RSSI of the third signal SF3 is detected and thus, the intermodulation signal for cancelling the RF signal distortion via the signal canceller 219 is detected. Fourthly, the RSSI of the fourth signal SF4 is detected and the intermodulation signal included in the output signal of the linear power amplifier (which is output in the main power amplifier 214 on the main path) can be controlled to be suppressed.

FIGs. 11A to 11C show the spectrum of the signals resulting from the control of the attenuation and the phase of a signal according to FIG. 10. FIG. 11A represents the second signal, SF2, that is, the output of the main power amplifier 214, that output being derived from the signal coupler 232. FIG. 11B represents the third signal SF3 derived from the signal coupler 233. FIG. 11C represents the fourth signal SF4 derived from output signal of the linear power amplifier via the signal coupler 224.

With reference to FIGs. 10 and 11, upon power-up, the controller 237 performs the initialization operation of the linear power amplifier as per step 1000. Upon initialization the CPU 811 reads the voltage values of the attenuation control signals ATT1 to ATT3 and the phase control signals PIC1 to PIC3 with the specific power and the specific frequency, stores the read voltage values in a corresponding area of the RAM 813, and initializes corresponding areas of the RAM 813 for storing the RSSI value corresponding the number of the transmitting channels and the service channel information. The initialization operation as above is performed only upon power-up of the linear power amplifier. Also, once the linear power amplifier is initialised, the initialization operation is not performed again until a subsequent power-up.

When the initialization operation is completed, the CPU 811 outputs the switch control signal SWC for selection of the first signal SF1 output from the power divider 231 in order to determine the service channel in step 1011 and outputs the control data PCD for selection of the first channel of the transmitting band in step 1013. In this case the signal selector 235 selectively outputs the first signal SF1 according to the switch control signal SWC and the signal detector 236 detects the RSSI for the first channel frequency according to the control data PCD. Thereafter, the controller 237 stores the RSSI received for the set channel in the corresponding channel area of the RAM 813 in step 1015 and increases the channel number in order to detect the RSSI of the next channel in step 1017. The channel scanning operation repeatedly performing steps 1011 to 1019 as described above is performed until the last channel of the transmitting band has been processed.

With reference to the channel scanning operation performed as above, the controller 237 detects the RSSI determined for each channel and stores the detected RSSI while sequentially increasing the channel number from the first channel to the final channel with respect to the total channels of the transmitting band. In the case where the present invention is used within the context of a mobile communication system which uses code division multiplexing access (hereinafter, referred to as CDMA), the transmitting band is 869.640MHz to 893.19MHz and the channel interval is 1.23MHz. Thus, in the case of the CDMA system, the band of the first signal SF1 is 869.640MHz to 893.19MHz, the control data PCD designates the first signal SF1 from the first channel frequency, 869.640MHz, to the 20th channel frequency, 893.10MHz, in intervals of 1.23MHz, in a sequential manner. In the CDMA system as mentioned previously, the controller 237 detects the RSSI of the designated channel and stores the detected RSSI in the RAM 813 while orderly designating each channel frequency of the transmitting band of 869.640MHz to 893.19Mz in the channel scanning operations.

When the channel scanning operation is finalized, the controller 237 summarizes the RSSI of the overall channels which are stored in the RAM 813 in step 1021 and calculates the average value by dividing the summarized value of the RSSI of the overall channels by the number of the channels in step 1023. Following that, while performing steps 1015 to 1035, the controller 237 determines the service channels. Regarding the steps for determining the service channel, the controller 237 accesses the RSSI values of each channel stored in the RAM 813 in an orderly manner and compares the accessed value with the averaged value. Then, upon checking, in step 1027, that the RSSI of the channel is greater than the averaged value, the controller 237 checks in step

1029, whether or not the RSSI value of the corresponding channel is greater than a reference value $+\alpha$. Herein, it is assumed that α = 3dB. Thus, if the RSSI value of the present channel is greater than the average value and the reference value in the aforesaid steps 1027 and 1029, the controller 237 checks in step 1029, whether or not the RSSI value of the corresponding channel is more than 30dB greater than the reference value $+\alpha$. This is to set those channels having a high signal distortion as service channels even if the detected RSSI value is greater than the average value. When the RSSI value of the present channel is greater than both the average value and the reference value $+\alpha$, the controller 237 sets the corresponding channel as a service channel in step 1031. While repeatedly performing steps 1025 to 1035, the controller 237 checks the size of the RSSI for all channels and sets the service channels accordingly.

After selecting the first signal SF1 as described hereinabove, the controller 237 detects and analyzes the RSSI value of all channels of the band of the first signal SF1, and sets and stores the channel to be transmitted and serviced. Thereafter, the controller 237 amplifies and outputs the RF signals of the set service channels. However, for convenience of the explanation, two sequential channels are serviced in the embodiment of the present invention. The frequencies of the RF signal of each channel are assumed to be f1 and f2, and the intermodulation signal is assumed as IM1 to IM2.

In FIG. 10, through steps 1111 to 1163, the controller 237 checks the intermodulation signal included in the output of the main power amplifier 214 and controls the variable attenuator 315 and the variable phase shifter 316. The predistortor 213 generates the predistortion signal for suppression of the intermodulation signal capable of being generated in the main power amplifier

214, and the controller 237 detects the RSSI of the intermodulation signal included in the output of the main power amplifier 214 and variably controls the phase and the attenuation level of the predistortion signal, so that the intermodulation signal can be smoothly suppressed in the main power amplifier 214. In the embodiment of the present invention, after detecting the RSSI of the intermodulation signal output by the main power amplifier 214, it is assumed that the controller 237 compares the detected values of the RSSI of the intermodulation signal with those of the previous RSSI intermodulation signal values, and performs control operations in three stages according to the compared results. Here, it is assumed that the ADC 814 and the DAC 815 are 16 bit converters, the first stage comprises three steps, the second stage comprises ten steps, and the third stage comprises 20 steps. A step represents a quantization step of the A/D conversion. During the time when the initial attenuation level and phase is controlled, the controller 237 increases the phase and the attenuation control signal by 1 step and the RSSI of the IM signal is detected from the second control operation to Xth control operation. The controller 237 controls the attenuation level and the phase of the first stage in the case when the comparison difference is below ten steps, controls the attenuation level and the phase of the second step in the case when the comparison difference is less than 20 steps, controls the attenuation level and phase of the third step in the case when the comparison difference is above 20 steps. As mentioned above, the operation of controlling the attenuation level and the phase of the predistortion signal is consecutively performed X times.

The controller 237 outputs the switch control signal SWC for selection of the second signal SF2 in step 1111. Thus, the signal selector 235 selects the signal as shown

in FIG. 11A at which is output from the main power amplifier 214, thereby outputting the selected signal to the signal detector 236. The controller 237 checks in step 1113, whether or not the value of the HG count is set as 0. At this time, the HG count counts the suppressed number of intermodulation signals contained in the main power amplifier 214. Here, when the value of the HG count is set to 0, the controller 237 outputs a phase control signal PIC3 derived from the previous phase control signal, PPIC3, + 1 step value, that is PIC3=PPIC3+1, in step 1115, and converts the phase control signal PIC3 into an analog signal by the DAC6 of the DAC 815 and then applies the analog signal to the variable attenuator 316. Thus, the variable attenuator 316 of the predistortor 213 adjusts the phase of the predistortion signal output from the harmonics generator 314 via the phase control signal PIC3 and couples the adjusted signal to the input terminal of the main power amplifier 214. In step 1117, the controller 237 stores the phase control signal PIC3 as the previous phase control signal, PPIC3, for the next iteration. Also, the controller 237, in step 1119, outputs an attenuation control signal ATT3 derived from the previous attenuation control signal, PATT3, + 1 step value, that is, ATT3=PAT13+1,and converts the attenuation control signal ATT3 into the analog signal by the DAC5 to be applied to the variable attenuator 315. At this point, the variable attenuator 315 of the predistortor 213 adjusts the level of the predistortion signal output by the harmonics generator 314 according to the attenuation control signal ATT3 and couples, via the variable phase shifter 316, the adjusted level to the input terminal of the main power amplifier 214. Following that, the controller 237 stores the attenuation control signal ATT3 as the previous attenuation control signal PATT3 in step 1121, in preparation for the next iteration or state.

It can be seen that the first phase and level controlling of the predistortion signal as stated above is performed by adding one step to the control signal of the previous state. However, the corresponding control signal can be determined by comparing the difference between the present detected control signal and the control signal of the previous state. After controlling the phase and the level of the predistortion signal as described above, the controller 237 increases the HG count in step 1161.

After controlling the phase and the level of the predistortion signal as described hereinbefore, the controller 237 again performs steps 1123 to 1135, detects the RSSIs of the intermodulation signals IM1 to IM4 included in the output of the main power amplifier 214 and selects the intermodulation IM having the greatest RSSI value in step 1139.

In order to achieve the above, the controller 237 sequentially outputs the control data PCD for selecting the signals IM1 to IM4 of the intermodulation signals in the output of the main power amplifier 214 to be output from the signal detector 236 as shown in FIG. 11A, and receives and stores each RSSI value of the corresponding intermodulation signals, IM1 to IM4.

As step 1139, the intermodulation signal having the greatest RSSI is selected.

Following that, in step 1141 the controller 237 compares the RSSI of the selected IM signal with the phase control signal PPIC3 of the previous state. If the IM signal is more than the phase control signal PPIC3, the controller 237 sets the phase control value to be decreased in step 1143 and, if the IM signal is less than the phase control signal PPIC3, the controller 237 sets the phase control value to be increased in step 1145. After setting the

increase/decrease direction of the phase control, the controller 237 obtains the difference between the value of the IM signal and the phase control signal PPIC3 of the previous state in step 1147, thereby generating the phase control signal PIC3 according to the above subtraction. The phase control signal PIC3 is applied to the variable phase shifter 316 through the DAC6 815. Thereafter, the controller 237 stores the phase control signal PIC3 as the previous phase control signal PPIC3 to be used in the next state.

In addition, after generating the phase control signal PIC3 as explained above, the controller 237 compares the RSSI of the selected IM signal with the attenuation control signal PATT3 of the previous state in step 1151. If the IM signal is more than the previous attenuation control signal PATT3, the controller 237 sets the attenuation control value to be decreased in step 1153. If the IM signal is less than the previous attenuation control signal PATT3, the controller 237 sets the attenuation control value to be increased in step 1155. After setting the increase/decrease direction of the attenuation control as described above, the controller 237 obtains the difference between the value of the selected IM signal and the attenuation control signal PATT3 of the previous state in step 1157, thereby generating the attenuation control signal ATT3 according to the above subtraction. The attenuation control signal ATT3 is applied to the variable attenuator 315 through the DAC 815. Thereafter, the controller 237 stores the attenuation control signal ATT3 as the previous attenuation control signal PATT3 in step 1159.

In step 1161, the controller 237 increases the HG count by one and thus, checks whether or not the HG count is still less than the value of X. If the HG count does not become the X value, the controller 237 returns to the

aforesaid step 1071, thereby repeatedly performing the above steps. While repeating the above steps, the controller 237 detects the RSSI of the intermodulation signal contained in the output of the main power amplifier 214 and thus, adjusts the phase and the attenuation level of the predistortion signal by comparing the phase and attenuation control signals PIC and ATT and determining the control direction and the control size. Here, the predistortion signal is applied as the anti-phase signal of the intermodulation signal to be generated to the main power amplifier 214. At the same time as adjusting the phase and the attenuation level of the predistortion signal, the controller 237 prevents the generation of the intermodulation signal and, if the HG count becomes X, completes the operation of adjusting the predistortion signal.

After adjusting the phase and the attenuation level of the predistortion signal, the controller 237 performs the operation to suppress the RF signal distortion included in the output of the signal canceller 219.

In FIG. 10, the controller 237 detects, in steps 1211 to 1255, the RF signal distortion pertaining to the output of the signal canceller 219 and controls the first variable attenuator 211 and the first variable phase shifter 212 accordingly. The signal canceller 219 cancels the output of the main power amplifier 214 as shown in FIG. 11A and the input RF signal, and extracts only the intermodulation signal generated upon amplification. At this point, the controller 237 detects the RSSI of the RF signal included in the output of the signal canceller 219 as shown in FIG. 11B and variably controls the attenuation level and the phase of the RF signal so as to suppress smoothly the RF signal in the signal canceller 219. In the embodiment of the present invention, after detecting the RSSI of the RF signal

(intermodulation signal) output by the signal canceller 219, the controller 237 compares the detected value with the RSSI of the RF signal of the previous state and performs the control operation, which includes three steps, depending on the comparison difference. Herein, when it is assumed that the ADC 814 is the 16 bit converter the first stage comprises as three steps, the second stage comprises ten steps, and the third stage comprises 20 steps. The steps represent the quantization steps of the A/D conversion process. At the point when the phase and the attenuation level are initially controlled, the controller 237 controls the phase and the attenuation level as the first step regardless of the detected RSSI; controls the phase and attenuation level of the first step in the case when the comparison difference is below ten steps, controls the phase and attenuation level of the second step in the case when the comparison difference is below 20 steps, controls the phase and attenuation level of the third step in the case when the comparison difference is above 20 steps. As mentioned above, the operations of controlling the attenuation level and the phase of the predistortion signal are consecutively performed in X times.

The controller 237 outputs the switch control signal SWC for selection of the third signal SF3 in step 1221. Thus, the signal selector 235 selects the signal as shown in FIG. 11A which is output from the signal canceller 219, thereby outputting the selected signal to the signal detector 236. Hereafter, the controller 237 detects and analyzes the RSSI of the intermodulation signal included in the output of the signal canceller 219, controls the first variable attenuator 211 and the first variable phase shifter 212 and adjusts the attenuation level and the phase of the RF signal.

In order to achieve the above, the controller 237 checks in step 1213 whether or not the sub count is set to 0. Herein, the sub count counts the number of the cancelled RF signal included in the signal canceller 219. If the value of the sub count is set to 0, the controller 237 outputs the phase control signal PIC1 as the previous phase control signal, PPIC1, + 1 step, ie PIC1=PPIC1+1, and stores PIC1 as PPIC1 in step 1215, and converts the phase control signal PIC1 into an analog signal, via the DAC2 of the DAC 815, to be applied to the first variable phase shifter 212. Thus, the first variable phase shifter 212 adjusts the phase of the input RF signal according to the phase control signal PIC1 and outputs the adjusted phase to the main power amplifier 214. Further, in step 1217, the controller 237 stores the phase control signal PIC1 as the previous phase control signal PPIC1 for the next state. Furthermore, the controller 237 outputs the attenuation control signal ATT1 as the attenuation control signal PATT1 + 1 step of the previous state in step 1219, and converts the attenuation control signal ATT1 into the analog signal, via the DAC1, to be applied to the variable attenuator 211. The controller 237 then stores the attenuation control signal ATT1 as the previous attenuation control signal PATT1 in preparation for the next iteration in step 1221. Thus, the first variable attenuator 211 adjusts the level of the input RF signal according to the attenuation control signal ATT1 and outputs the adjusted level, via the first variable phase shifter 212, to the main power amplifier 214.

The first phase and attenuation level of the RF signal as stated above is controlled by adding one step to the control signal of the previous state. However, the corresponding control signal can be determined by comparing the difference between the present detected control signal and the control signal of the previous

state. After controlling the phase and the attenuation level of the RF signal as described above, the controller 237 increases the SUB count in step 1253.

To the contrary, when checking in step 1213 that the SUB count is set to 0, the controller 237 sequentially outputs the control data PCD for selecting signals f1 to f2 in the output of the signal canceller 219 as shown in FIG. 11B, and receives and stores the RSSI values of the corresponding signals f1 to f2. The controller 237 selects the f signal having the greatest RSSI value among the f1 to f2 signals in step 1231.

Following that, the controller 237 compares the RSSI of the selected f signal with the previous phase control signal PPIC1 of the previous state in step 1233. At this time, if the f signal is more than the previous phase control signal PPIC1, the controller 237 sets the phase control value to be decreased in step 1235 and, if the f signal is less than the phase control signal PPIC1, the controller 237 sets the phase control value to be increased in step 1237. After setting the increase/decrease direction of the phase control signal, the controller 237 obtains the difference between the value of the f signal and the previous phase control signal PPIC3 in step 1239, thereby generating the phase control signal PIC1 according to the above subtraction. The phase control signal PIC1 is applied to the first variable phase shifter 212 through the DAC 815. Thereafter, the controller 237 stores the phase control signal PIC1 as the previous phase control signal PPIC1 to be used in the next state in step 1241.

In addition, after generating the phase control signal PIC1, the controller 237 compares, in step 1243, the RSSI of the selected f signal with the value of the attenuation control signal PATT1 of the previous state.

If the f signal is less than the previous attenuation control signal PATT1, the controller 237 sets the attenuation control value PATT1 to be decreased in step 1245 and, if the f signal is more than the attenuation control signal PATT1, the controller 237 sets the attenuation control value PATT1 to be increased in step 1247. After setting the increase/decrease direction of the attenuation control, the controller 237 obtains the difference between the value of the f signal and the attenuation control signal PPIC1 of the previous state in step 1249, thereby generating the attenuation control signal ATT1 according to the above subtraction. The attenuation control signal ATT1 is applied to the first variable attenuator 211 through the DAC 815. Thereafter, in step 1251, the controller 237 stores the attenuation control signal ATT1 as the previous attenuation control signal PATT1.

After increasing the SUB count by one in step 1253, the controller 237 checks in step 1255 whether or not the SUB count is less than the value Y. If the SUB count is less than the Y value, the controller 237 returns to step 1223, thereby repeatedly performing the above steps. While repeating the above steps, the controller 237 detects the RSSI of the RF signal contained in the signal canceller 219 and thus, adjusts the phase and the attenuation level of the RF signal by comparing the RSSI of the RF signal output from the signal canceller 219 with the previous state and determining the control direction and the control size accordingly. While adjusting the phase and the attenuation level of the input RF signal as above, the controller 237 prevents the generation of the RF signal pertaining to the signal and, if the SUB count becomes Y, completes the operation of suppressing the RF signal included in the signal canceller 219.

In FIG. 10, the controller 237 detects, in steps 1311 to 1363, the intermodulation signal IM included in the RF signal which is finally output by the linear power amplifier 214 and controls the second variable attenuator 220 and the second variable phase shifter 221 accordingly. The RF signal output by the main power amplifier 214 is delayed through the second delay 215 during the processing of the intermodulation signal detected in the sub path. The intermodulation signal distortion included in the RF signal which is finally output is coupled by the signal coupler 223 with the anti-phase signal of the intermodulation distortion processed in the sub path can be suppressed. In this case, the intermodulation signal distortion can be included in the RF signal which is finally output and the included intermodulation distortion can not avoid being suppressed.

The controller 237 detects the RSSI of the intermodulation signals IM1 to IM4 included in the output of the linear power amplifier 214 as shown in FIG. 11C and variably controls the phase and the attenuation level of the intermodulation signals IM1 to IM4, in order that the intermodulation signal distortion pertaining to the RF signal which is finally output by the signal coupler 223, can be smoothly suppressed in the main power amplifier 214. In the embodiment of the present invention, after detecting the RSSI of the intermodulation signals IM1 to IM4 contained in the RF signal amplified and finally output, it is assumed that the controller 237 compares the detected value with the RSSI of the intermodulation signals IM1 to IM4 of the previous state, and performs a control operation comprising three stages according to the compared results. Herein, it is assumed that the ADC 814 is a 16 bit converter, the first stage comprises three steps, the second stage comprises ten steps, and the third stage

comprises 20 steps. Each step represents the quantization step of an A/D conversion process. During the time when the initial attenuation level and phase are controlled, the controller 237 increases the phase and the attenuation control signal by 1 step and the RSSI of the IM signal is determined from the second control operation to the Xth control operation. The controller 237 controls the phase and attenuation level of the first step in the case when the comparison difference is below ten steps, controls the phase and attenuation level of the second step in the case when the comparison difference is below 20 steps and controls the phase and attenuation level of the third step in the case when the comparison difference is above 20 steps. As mentioned above, the operation of controlling the attenuation level and the phase of the predistortion signal is consecutively performed Z times.

As illustrated in FIG. 10, steps 1311 to 1363 are processed in the same order as that of the aforesaid step 1111 to 1163 for adjusting the attenuation level and the phase of the predistortion signal. Namely, the controller 237 controls the signal selector 235, selects the fourth signal SF4, controls the signal detector 236, and sequentially selects the intermodulation signal IM1 to IM4. Hereafter, the controller 237 sequentially receives the RSSIs of the intermodulation signals IM1 to IM4 detected in the signal detector 236. After selecting the intermodulation signal IM having the greatest RSSI in the received intermodulation signals IM1 to IM4, the controller 237 compares the RSSI of the present detected intermodulation signal IM with the corresponding intermodulation signal IM of the previous state. The controller 237 controls the second variable phase shifter 221 and the second variable attenuator 220 with obtaining the phase control signal PIC2 and the attenuation control signal ATT2 corresponding to the comparison difference

between the above intermodulation signals distortions. At this time, the controller 239 controls the second variable attenuator 220 and the second variable phase shifter 221 by Z times.

As shown in FIG. 10, the linear power amplifier according to the embodiment of the present invention sets the service channels and adjusts the attenuation level and the phase of the predistortion signal for suppression of the intermodulation signal included in the main power amplifier 214, in a sequential manner. Also, the above amplifier adjusts the phase and the attenuation level of the RF signal input in the main path for suppression of the RF signal contained in the signal canceller 219, and the attenuation level and the phase of the intermodulation signal output from the signal canceller 219, so that the intermodulation signal pertaining to the amplified and finally-output RF signal can be suppressed.

An example according to the embodiment of the present invention can be achieved by, firstly, selecting the service channels, secondly, controlling the phase and the attenuation level of the predistortion signal, thirdly, controlling the phase and the attenuation level of the input RF signal, and fourthly, controlling the phase and the level of the intermodulation signal output by the signal canceller 219. However, as another embodiment thereto, the operation of selecting the service channels can be performed at intervals of given times by a timer interrupt. In the case of using the above control method, the controller 237 performs the service channel seek operation whenever a timer interrupt is generated, and controls the variable attenuators and the variable phase shifters as noted above between interrupt periods. At this point, when a timer interrupt is generated in the state where an arbitrary variable attenuator and an arbitrary variable phase shifter are controlled, the

controller 237 interrupts the operation and performs the timer interrupt service routine, thereby again returning to the main routine and performing the operation which is currently being executed.

Further, with respect to FIG. 10, while the numbers, that is, X, Y, and Z by which the variable attenuators and the variable phase shifters are controlled, can be set to any number capable of effectively controlling the attenuation level and the phase of the input signal to corresponding variable attenuators and variable phase shifters, the numbers are preferably set to the same number and more particularly to the value 5.

FIG. 12 is a block diagram showing the construction of a linear power amplifier according to a second embodiment of the present invention. The linear power amplifier according a second embodiment of the present invention has the same construction as that according the first embodiment thereof, as shown in FIG. 1, except that the first variable attenuator 211 and the first variable phase shifter 212 are positioned in the sub path.

In connection with FIG. 12, the predistortor 213 on the main path has the same construction as that as shown in FIGs. 3 and 5, generates the harmonics corresponding to the input RF signal, controls the attenuation level and the phase of the harmonics depending on the attenuation control signal ATT3 and the phase control signal PIC3 of the controller 237, couples the controlled signals to the input RF signal, converts the coupled signals into the predistorted RF signal and outputs the converted signals to the main power amplifier 214. The main power amplifier 214 receives the output of the predistortor 213, amplifies the predistorted RF signal, and outputs the RF signal thereby suppressing intermodulation signal distortion.

The rest of construction of the linear power amplifier is identical to that in the first embodiment of the present invention as shown in FIG. 2, except for the above construction. Thus, the reference numerals of the second embodiment of the present invention correspond to those of the first embodiment thereof. Furthermore, the controller 237 selectively inputs the first signal SF1 to the fourth signal SF4 in the same manner as that of FIG. 10 and generates the attenuation control signals ATT1 to ATT3 and the phase control signals PIC1 to PIC3 with detection of the RSSI of the RF signal or the intermodulation signal in the selected SF signal. After setting the service channels, the controller 237 orderly adjusts the phase and the attenuation level of the predistortion signal for suppression of the intermodulation signal pertaining to the main power amplifier 214, adjusts the attenuation level and the phase of the input RF signal input in the sub path so as to suppress the RF signal distortion included in the signal canceller 219, and lastly adjusts the attenuation level and the phase of the intermodulation signal distortion output to the signal canceller 219 so as to suppress the intermodulation signal distortion pertaining to the amplified and finally-output RF signal of the linear amplifier.

FIG. 13 is a block diagram showing the construction of a linear power amplifier according to a third embodiment of the present invention. The linear power amplifier according a third embodiment of the present invention has the same construction as that according the second embodiment thereof, as shown in FIG. 13, except that the first variable attenuator 211 and the first variable phase shifter 212 are positioned between the main path and the sub path.

With regard to FIG. 13, the predistortor 213 on the main path has the same construction as that shown in FIGs. 3 and 5, generates the harmonics corresponding to the input RF signal, controls the attenuation level and the phase of the harmonics depending on the attenuation control signal ATT3 and the phase control signal PIC3 of the controller 237, couples the controlled signals to the input RF signal, converts the coupled signals into the predistorted signal, and lastly outputs the converted signal to the main power amplifier 214. The main power amplifier 214 receives the output of the predistortor 213 and outputs the RF signal thereby suppressing the intermodulation signal distortion by amplifying the predistorted RF signal.

The first delay 217 is located in the sub path and receives the RF signal of the main path via the power divider 216, delays the RF signal while the RF signal is processed by the predistortor 213 and the main power amplifier 214, and outputs the delayed RF signal to the signal canceller 219.

The first variable attenuator 211 and the first variable phase shifter 212 are connected between the power divider 218 and the signal canceller 219, which respectively control the attenuation level and the phase of the input RF signal according to the attenuation control signal ATT1 and the phase control signal PIC1 output by the controller 237 and outputs the controlled attenuation level and phase to the signal canceller 219. That is, the first variable attenuator 211 and the first variable phase shifter 212 are positioned between the main path and the sub path, and the phase and the attenuation level of the RF signal amplified and output by the main power amplifier 214 on the main path are controlled before being output to the signal canceller 219.

The rest of the construction of the linear power amplifier is identical to that in the first embodiment of the present invention as shown in FIG. 2, except for the above construction. Thus, the reference numerals of the third embodiment of the present invention are equal to those of the first embodiment thereof.

Furthermore, the controller 237 selectively inputs the first signal SF1 to the fourth signal SF4 in the same manner as that of FIG. 10 and generates the attenuation control signals ATT1 to ATT3 and the phase control signals PIC1 to PIC3 with detection of the RSSI of the RF signal or the intermodulation signal in the selected SF signal. After setting the service channels, the controller 237 orderly adjusts the phase and the attenuation level of the predistortion signal for suppression of the intermodulation signal pertaining to the main power amplifier 214, adjusts the attenuation level and the phase of the input RF signal in the sub path so as to suppress the RF signal distortion included in the signal canceller 219, and lastly adjusts the attenuation level and the phase of the intermodulation signal distortion output by the signal canceller 219 so as to suppress the intermodulation signal distortion pertaining to the amplified and finally-output RF signal.

Likewise, the linear power amplifier according to the first embodiment of the present invention, the linear power amplifiers according the second and third embodiments of the present invention, firstly select the service channel, secondly control the phase and the attenuation level of the predistortion signal, thirdly control the phase and the attenuation level of the input RF signal, and fourthly control the phase and the attenuation level of the intermodulation signal output by the signal canceller 219. On the contrary, as another embodiment thereto, the operation of selecting the

service channel can be performed during intervals of given times by the timer interrupt. In the case of using the above control method, the controller 237 performs the service channel seek operation whenever a timer interrupt is generated, and controls the variable attenuators and the variable phase shifters as noted above between interrupt periods. At this point, when a timer interrupt is generated in the state where an arbitrary variable attenuator and an variable phase shifter are being controlled, the controller 237 interrupts the operation and performs the timer interrupt service routine and then returns to the main routine and performing the operation which was currently being executed.

Moreover, with respect to FIG. 10, while the numbers, that is, X, Y, and Z, by which the variable attenuators and the variable phase shifters are controlled, can be set to any number capable of effectively controlling the attenuation level and the phase of the input signal to corresponding variable attenuators and variable phase shifters, the numbers are preferably set to the same number and more particularly are set to the value 5.

As may be apparent from the foregoing, the linear power amplifier according to the embodiment of the present invention effectively divides and controls the intermodulation signal distortion with the predistortion system and the feedforward system. In other words, the linear power amplifier firstly suppresses the intermodulation signal distortion capable of being generated in the main power amplifier by using the predistortion system and secondly suppresses the intermodulation signal pertaining to the output of the main power amplifier by using the feedforward system. In this manner, the design and manufacture of the main power amplifier 214 or the error amplifier 222 are improved. Likewise, since the variable attenuators and the variable

phase shifters performing the linearity function, have wide frequency bandwidths and relatively flat amplification or attenuation across those bandwidths, the linear power amplifier according to the present invention can be used for many purposes.

Therefore, it should be understood that the present invention is not limited to the particular embodiments disclosed herein as the best mode contemplated for carrying out the present invention, but rather that the present invention is not limited to the specific embodiments described in this specification except as defined in the appended claims.

CLAIMS:

1. A linear amplifier having an input for receiving an input RF signal, an output for outputting an amplified RF signal and a main amplifier which generates, in response to said amplification of said RF input signal, an intermodulation signal, said linear power amplifier having a main path and a sub-path via which said input RF is processed, said linear power amplifier comprising:

a predistortor for suppressing said intermodulation signal generated upon amplification of said input Rf signal, said predistortor comprising a harmonics generator for generating a harmonics signal corresponding to said input RF signal and for coupling said harmonics signal to said input RF signal to thereby produce a predistorted RF signal; and

a feedforward system comprising means for cancelling said input RF signal and said output of said main power amplifier to extract said intermodulation signal, means for error-amplifying said extracted intermodulation signal and for coupling said error-amplified intermodulation signal with the output of the main power amplifier.

2. A linear power amplifier as claimed in claim 1, wherein said predistortor comprises

a power divider for dividing power from said input RF signal,

an automatic level controller for controlling and outputting said divided RF signal at a given level,

a harmonics generator for generating harmonics signal corresponding to said level-controlled RF signal; and

a signal coupler for coupling said harmonics generator with said input RF signal to thereby produce a predistorted RF signal.

3. A linear power amplifier as claimed in either of claims 1 or 2, wherein said feedforward system comprises

a power divider for dividing said input RF signal between a main path and a sub-path of said linear power amplifier;

a signal canceller for cancelling said RF signal of the sub-path and the output of the main power amplifier to extract from said output of the main amplifier said intermodulation signal;

an error-amplifier for amplifying said extracted intermodulation signal output by said signal canceller;

a signal coupler for coupling the output of the error-amplifier with the output of the main power amplifier on said main path to thereby suppress said intermodulation signal in said output of the linear power amplifier.

4. A linear power amplifier as claimed in any preceding claim, further comprising

a third variable attenuator and phase shifter for adjusting the attenuation level and phase of said harmonics signal output by said harmonics generator;

a delay for delaying said input RF signal; and wherein

said signal coupler is arranged to receive said output of said harmonics generator after processing thereof via said third variable attenuator and phase shifter.

5. A linear power amplifier as claimed in any preceding claim, further comprising

a first variable attenuator and phase shifter positioned within said main path for adjusting the attenuation level and phase of said input RF signal; and wherein

said predistortor is arranged to receive said input RF signal via said first variable attenuator and phase shifter;

and further comprising

a main power amplifier for amplifying and outputting said predistorted signal;

a first delay positioned within said sub-path, for delaying said divided RF signal derived from said main path; the output of the first delaying is arranged to feed the signal canceller;

a second variable attenuator and phase shifter for adjusting the attenuation level and phase of said intermodulation signal output by said signal canceller; and wherein said error amplifier is arranged to amplifier the intermodulation signal after processing thereof by said second variable attenuator and phase shifter; and

a second delay for delaying the output of said main power amplifier; and

a signal coupler for coupling said intermodulation signal amplified by said error-amplifier with the output of the second delay to thereby suppress said intermodulation signal in the output of the linear power amplifier.

6. A linear power amplifier as claimed in any of claim 1 to 4, further comprising

a first delay for delaying said divided input RF signal before input to a first variable attenuator and phase shifter;

a first variable attenuator and phase shifter position within the sub-path for receiving from said first delay said divided input RF signal and adjusting the attenuation level and phase thereof; and

wherein said signal canceller is arranged to receive the main power amplifier output signal and the output of the first variable attenuation and phase shifter;

and further comprising

a second variable attenuator and phase shifter for adjusting the phase and attenuation level of said intermodulation product produced by said signal canceller;

an error-amplifier for amplifying said intermodulation signal output by said second variable attenuation and phase shifter;

a second delay for delaying the output of said main power amplifier; said signal coupler being arranged to couple said intermodulation signal output from said error-amplifier with said output of said second delay to thereby suppress said intermodulation signal in the output of said linear amplifier.

7. A linear amplifier as claimed in any of claims 1 to 4, further comprising

a first delay positioned within said sub-path for delaying an divided RF signal derived from said input RF signal of said main path;

a first variable attenuator and phase shifter positioned between said sub-path and said main path for receiving and adjusting the attenuation and phase of the output of the main power amplifier divided from the main path;

and wherein said signal canceller is arranged to receive the output of the first delay and the output of the first variable attenuator and phase shifter;

and further comprising

a second variable attenuator and phase shifter for adjusting the phase and attenuation level of said intermodulation product produced by said signal canceller;

an error-amplifier for amplifying said intermodulation signal output by said second variable attenuation and phase shifter;

a second delay for delaying the output of said main power amplifier; said signal coupler being arranged

to couple said intermodulation signal output from said error-amplifier with said output of said second delay to thereby suppress said intermodulation signal in the output of said linear amplifier.

8. A linear power amplifier as claimed in any preceding claim, further comprising

a controller for generating a first attenuation control signal and a first phase control signal; and wherein

said first variable attenuator and phase shifter is arranged to adjust the attenuation level and the degree of phase shift according to the first attenuation control signal and the first phase control signal.

9. A linear power amplifier as claimed in any preceding claim, further comprising

a controller for generating a second attenuation control signal and a second phase control signal; and wherein

said second variable attenuator and phase shifter is arranged to adjust the attenuation level and the degree of phase shift according to the second attenuation control signal and the second phase control signal.

10. A linear power amplifier as claimed in any preceding claim, further comprising

a controller for generating a third attenuation control signal and a third phase control signal; and wherein

said predistortor is arranged to adjust the attenuation level and degree of phase shift according to the third attenuation control signal and the third phase control signal.

11. A linear power amplifier as claimed in any preceding claim, further comprising

a controller for generating a switch control signal for sequentially selecting one of a plurality of signal to be processed, and for generating control data for synchronising the frequencies of the input RF signal and the intermodulation signal;

a signal selector including four power dividers, two of which divide the output of the main power amplifier, one of which divides the output of the signal canceller, and the remaining power divider divides the input RF signal, said signal selector comprising means for selectively outputting a selectable one of said four divided signals according to said switch control signal; and

a signal detector for receiving the output of the signal selector, synchronising the frequencies of the input RF signal and the intermodulation signals according to control data and for determining a received signal strength indicator (RSSI) therefor.

12. A linear power amplifier as claimed in claim 11, wherein said controller further comprises

means for comparing RSSI of said intermodulation signal output from said signal detector with RSSI of an intermodulation signal of a previously state or previously stored RSSI, generating said third attenuation control signal and said third phase

control signal according to said compared result, outputting said control data for synchronization of said RF signals pertaining to the output of said signal canceller upon selecting the output of said signal canceller, comparing the RSSI of said RF signals output by said signal detector with the RSSI of said RF signal of the previous state, and generating said first attenuation control signal and said first phase control signal according to the compared result, generating said control data for synchronization of said intermodulation signals contained in said RF signal upon selecting said the output RF signal of said linear power amplifier, comparing the RSSI of said intermodulation signals output by said signal detector with the RSSI of said intermodulation signal of the previous state, and generating said second attenuation control signal and said second phase control signal according to the compared result.

13. A linear power amplifier as claimed in any preceding claim, further comprising

a phase locked loop for generating a selectable local frequency;

a mixer for mixing the signal output from the signal selector with the local frequency;

a filter for performing frequency down conversion of the output of said mixer; and

a log amplifier for converting the output of said filter into a voltage signal and outputting the voltage signal as an indication of the RSSI.

14. A method for eliminating an intermodulation signal of a linear power amplifier comprising the steps of

(a) generating a harmonics signal corresponding to said input RF signal, coupling said harmonics signal to said input RF signal to thereby produce a predistorted RF signal; and

(b) suppressing said intermodulation signal by cancelling said input RF signal and said output of said main power amplifier to extract said intermodulation signal, error-amplifying said extracted intermodulation signal, and coupling said error-amplified intermodulation signal with the output of the main power amplifier.

15. A method as claimed in claim 14, wherein step (a) further comprises the steps of

dividing said input RF signal and maintaining said divided input RF signal at a constant level;

generating a harmonics signal corresponding to said input RF signal:

coupling said harmonics signal with said input RF signal to thereby generate a predistortion RF signal; and

firstly suppressing an intermodulation signal using said predistortion signal.

16. A method as claimed in either of claims 14 or 15, wherein said step (b) further comprises the steps of:

cancelling said firstly-suppressed main amplifier output signal and said input RF signal and extracting said intermodulation signal;

amplifying said extracted intermodulation signal; and

secondly suppressing said intermodulation signal contained in the output of said linear power amplifier by coupling said amplified intermodulation signal to said firstly-suppressed main amplifier output signal.

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H3W WUL

Int Cl (Ed.6): H03F 1/32

Other: ONLINE:WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X,Y	EP 0411180 A1	(NIPPON)	1-4,14-16 (X) 6(Y)
X,Y	WO 91/07813 A1	(MOTOROLA)	1-5,8,9,14-16 (X) 6(Y)
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